CS1621

RAM Mapping 32×4 LCD Controller for I/O µC

1、GENERAL DESCRIPTION

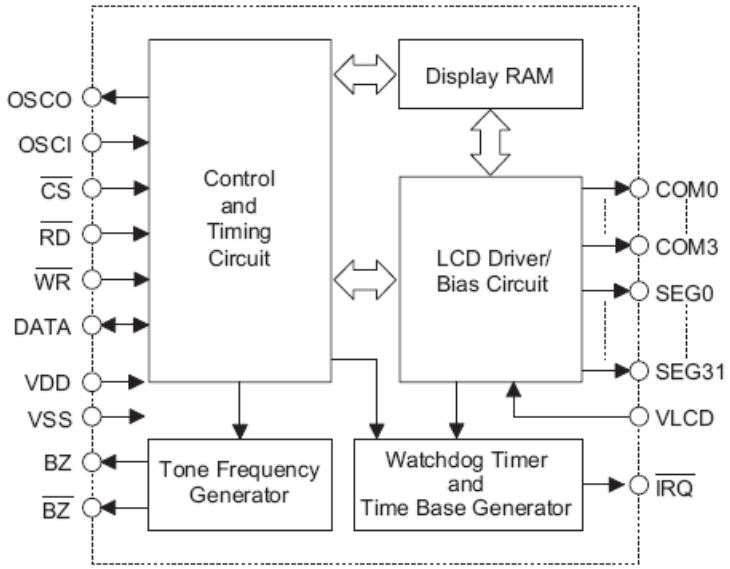
The CS1621 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the CS1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the CS1621. The CS1621 contains a power down command to reduce power consumption.

Features

- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- Chip size: 1690×1910(µm×µm).
- The IC substrate should be connected to V_{DD} or float in the PCB layout artwork.
- SSOP48 or bare chip available

2、BLOCK DIAGTAM AND PIN DESCRIPTION

2.1、BLOCK DIAGTAM



Note: $\overline{CS}$: Chip selection

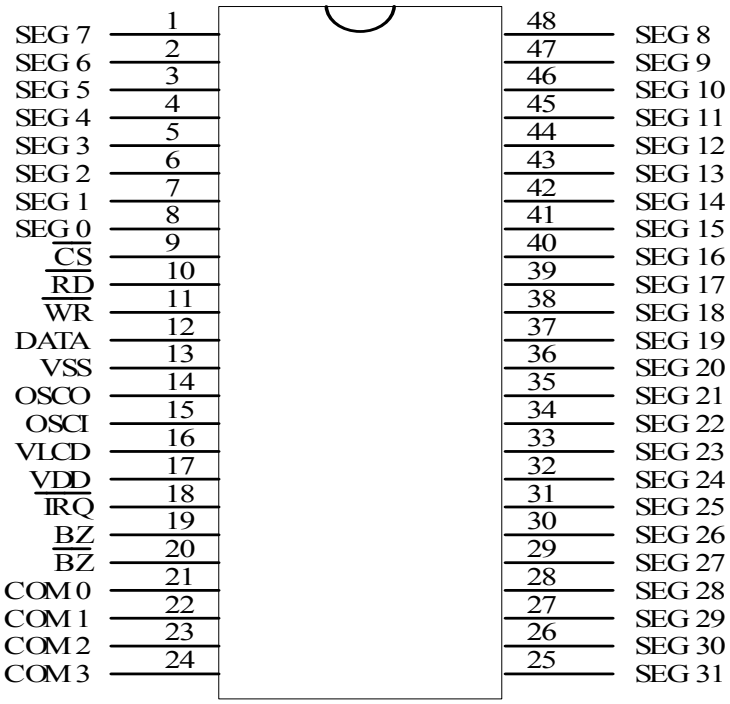
BZ, $\overline{BZ}$: Tone outputs

$\overline{WR}$, $\overline{RD}$, DATA: Serial interface

COM0~COM3, SEG0~SEG31: LCD outputs

$\overline{IRQ}$: Time base or WDT overflow output

2.2、PIN CONFIGURATIONS



2.3、PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
9	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the CS1621 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the CS1621 are all enabled.
10	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the CS1621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
11	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the CS1621 on the rising edge of the $\overline{WR}$ signal.
12	DATA	I/O	Serial data input/output with pull-high resistor
13	VSS	-	Negative power supply, ground
14	OSCO	O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
15	OSCI	I	
16	VLCD	I	LCD power input
17	VDD	P	Positive power supply
18	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
19，20	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
21~24	COM0~COM3	O	LCD common outputs
1~8 25~48	SEG0~SEG31	O	LCD segment outputs

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
Power Supply Voltage	VDD		-0.3～5.5	V
Input Voltage	VIN		V_{SS}-0.3～V_{DD}+0.3	V
Operating Temperature	Topr		-25～70	℃
Storage Temperature	Tstg		-50～125	℃
Soldering Temperature	T_L	10s	245	℃

3.2、ELECTRICAL CHARACTERISTICS

3.2.1、D.C. Characteristics (Tamb=25°C , unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	-	-	2.4	-	5.2	V
IDD1	Operating Current	3V	No load/LCD ON On-chip RC oscillator	-	150	300	uA
		5V		-	300	600	uA
IDD2	Operating Current	3V	No load/LCD ON Crystal oscillator	-	60	120	uA
		5V		-	120	240	uA
IDD3	Operating Current	3V	No load/LCD ON External clock source	-	100	200	uA
		5V		-	200	400	uA
ISTB	Standby Current	3V	No load, Power down mode	-	0.1	5	uA
		5V		-	0.3	10	uA
VIL	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	-	0.6	V
		5V		0	-	1.0	V
VIH	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	-	3.0	V
		5V		4.0	-	5.0	V
IOL1	DATA, BZ, BZ, IRQ	3V	VOL=0.3V	0.5	1.2	-	mA
		5V	VOL=0.5V	1.3	2.6	-	mA
IOH1	DATA, BZ, BZ	3V	VOH=2.7V	-0.4	-0.8	-	mA
		5V	VOH=4.5V	-0.9	-1.8	-	mA
IOL2	LCD Common Sink Current	3V	VOL=0.3V	80	150	-	uA
		5V	VOL=0.5V	150	250	-	uA
IOH2	LCD Common Source Current	3V	VOH=2.7V	-80	-120	-	uA
		5V	VOH=4.5V	-120	-200	-	uA

IOL3	LCD Segment Sink Current	3V	VOL=0.3V	60	120	-	uA
		5V	VOL=0.5V	120	200	-	uA
IOH3	LCD Segment Source Current	3V	VOH=2.7V	-40	-70	-	uA
		5V	VOH=4.5V	-70	-100	-	uA
RPH	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kW
		5V		30	60	100	kW

3.2.2、A.C. Characteristics (Tamb=25°C , unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
f_{SYS1}	System Clock	-	On-chip RC oscillator	-	256	-	kHz
f_{SYS2}	System Clock	-	Crystal oscillator	-	32.768	-	kHz
f_{SYS3}	System Clock	-	External clock source	-	256	-	kHz
f_{LCD}	LCD Clock	-	On-chip RC oscillator	-	fSYS1/1024	-	Hz
		-	Crystal oscillator	-	fSYS2/128	-	Hz
		-	External clock source	-	fSYS3/1024	-	Hz
t_{COM}	LCD Common Period	-	n: Number of COM	-	n/fLCD	-	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	-	-	150	kHz
		5V		-	-	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	-	-	75	kHz
		5V		-	-	150	kHz
f_{TONE}	Tone Frequency	-	On-chip RC oscillator	-	2.0 or 4.0	-	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	-	CS	-	250	-	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	-	-	us
			Read mode	6.67	-	-	
		5V	Write mode	1.67	-	-	us
			Read mode	3.34	-	-	
tr,tf	Rise/Fall Time Serial Data Clock Width (Figure 1)	–		–	120	-	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	–	–	–	120	-	ns
t_h	Hold Time for DATA to $\overline{WR}$,	–	–	–	120	-	ns

	$\overline{RD}$ Clock Width (Figure 2)						
t_{su1}	Setup Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	–	–	–	100	-	ns
t_{h1}	Hold Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	–	–	–	100	-	ns

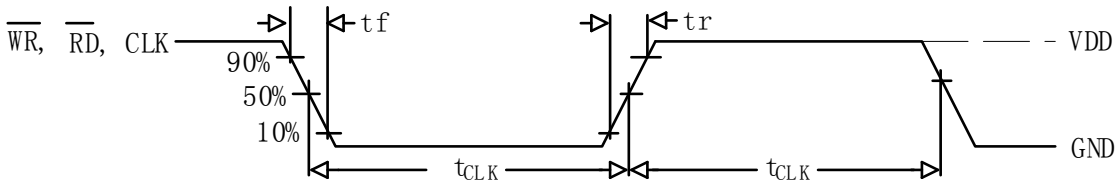


Figure 1

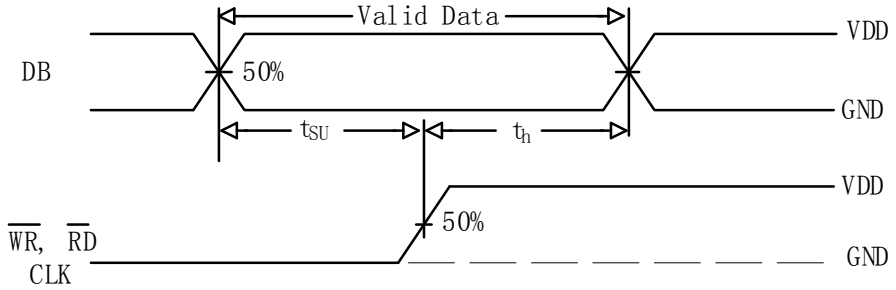


Figure 2

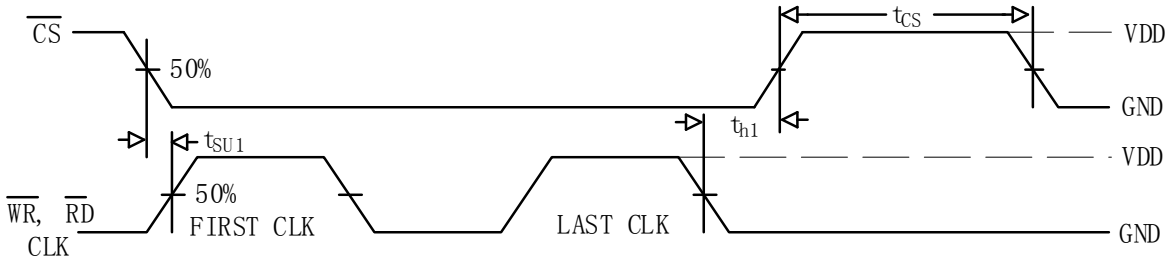
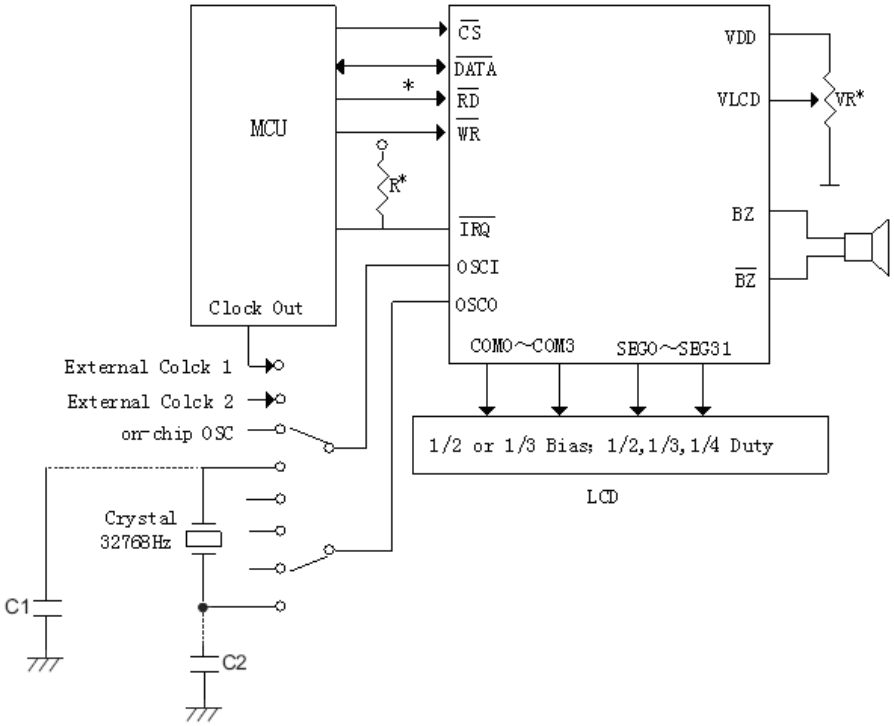


Figure 3

4、TYPACAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ RD pin can be selected depending on the requirement of the MCU.

The voltage applied to VLCD pin must be lower than VDD.

Adjust VR to fit LCD display, at VDD=5V, VLCD=4V, VR=15kΩ±20%.

Adjust R (external pull-high resistance) to fit user's time base clock.

For best performance , needing to add two load capacitances(C1 and C2).the value of capacitance will effect the oscillator accuracy.

Recommend the value of capacitance :

Oscillator's accuracy	Capacitance's value
±10ppm	0~10p
10~20ppm	10~20p

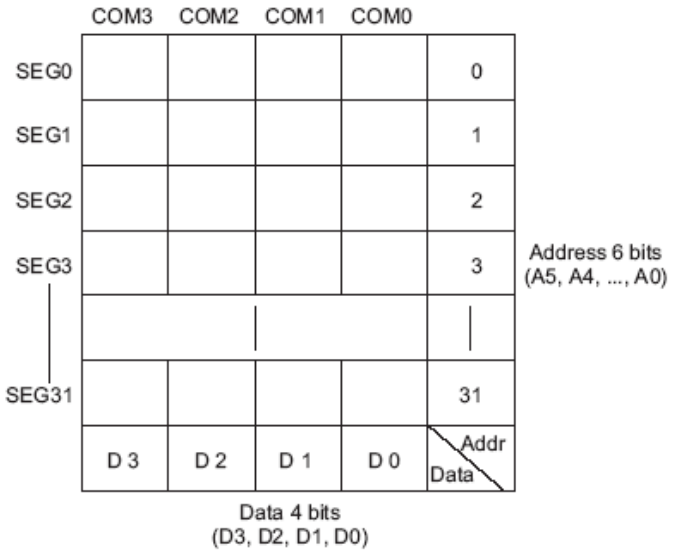
4. 2、FUNCTION DESCRIPTION

The CS1621 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. Only three or four lines are required for the interface between the host controller and the CS1621.

It will be cleared once power on, than can be set up the operating status by command port. Through the select port、read port and write port of the CS1621 will read、write and modify the data of RAM, the contents of the RAM and LCD display is corresponding. The CS1621 is a dot matrix LCD driver, each SEG port is independent , and easy to modify the RAM data .so displaying flexible contents, the users may be customized it according to the needs.

1）Display Memory －RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:

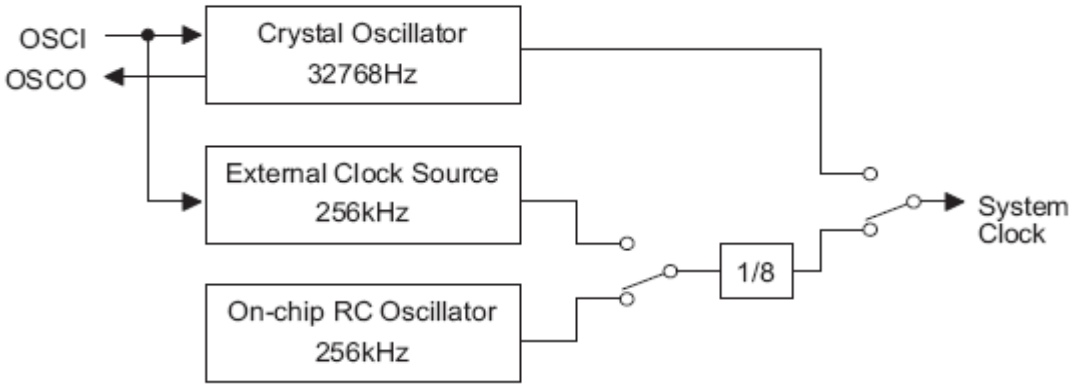


RAM Mapping

2）System Oscillator

The CS1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the CS1621 is at the SYS DIS state.



System Oscillator Configuration

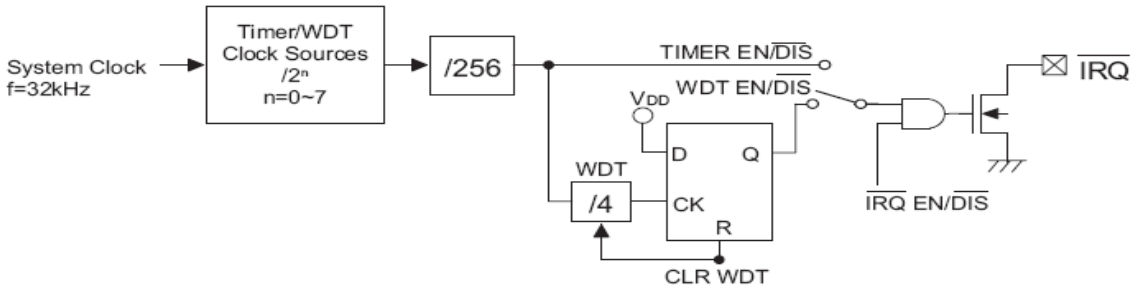
3）Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the IRQ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT} = \frac{32kHz}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command



Timer and WDT Configurations

not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the CS1621 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

4）Tone Output

A simple tone generator is implemented in the CS1621. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

5）LCD Driver

The CS1621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the CS1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator

frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator.

The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the CS1621 can be compatible with most types of LCD panels.

Name	Command Code	Function
LCD OFF	**100** 00000010X	Turn off LCD outputs
LCD ON	**100** 00000011X	Turn on LCD outputs
BIAS & COM	**100** 0010abXcX	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

6）Command Format

The CS1621 can be configured by the S/W setting. There are two mode commands to configure the CS1621 resources and to transfer the LCD display data. The configuration mode of the CS1621 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and

READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to “1” and the previous operation mode will be reset also. Once the CS pin returns to “0” a new operation mode ID should be issued first.

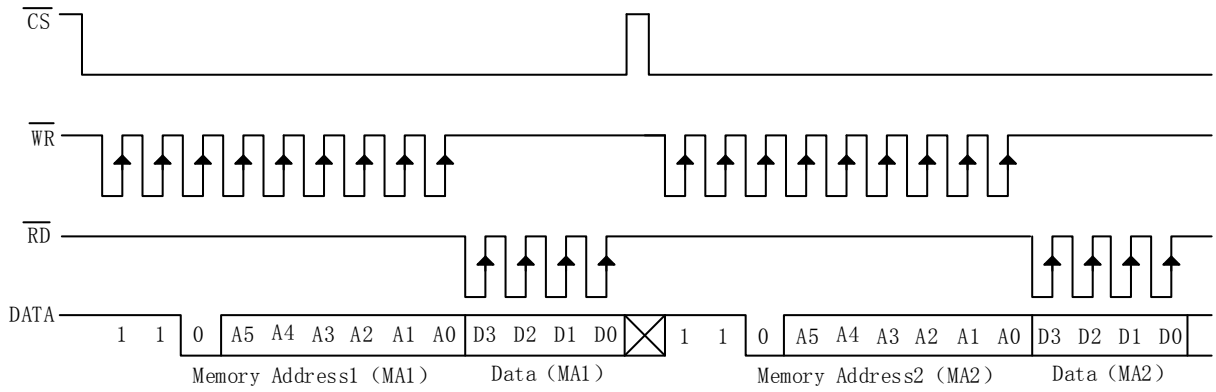
7）Interfacing

Only four lines are required to interface with the CS1621. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the

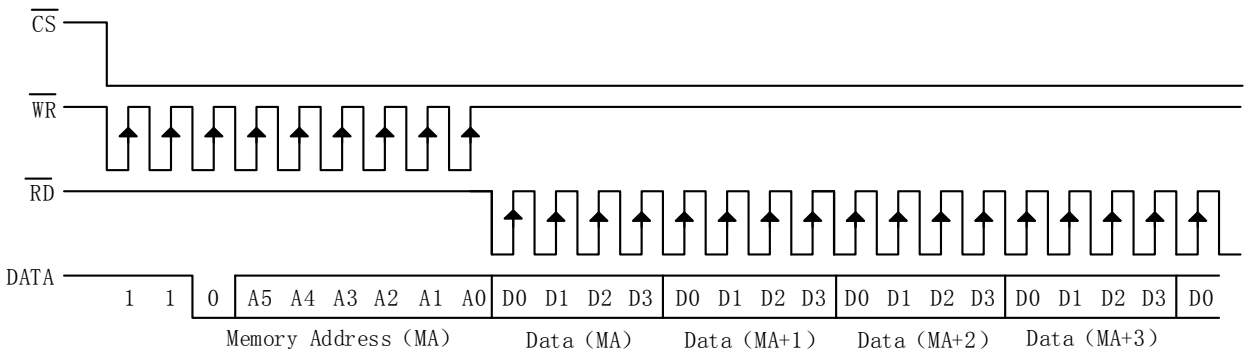
CS1621. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the CS1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the CS1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the CS1621 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the CS1621. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the CS1621.

8）Timing Diagrams

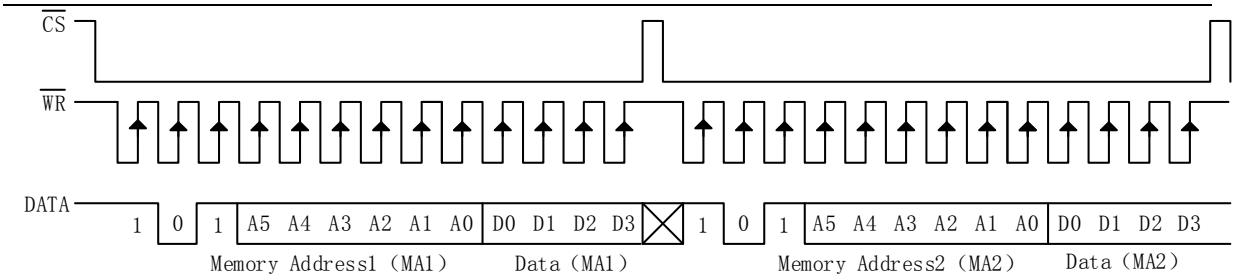
a. READ Mode (Command Code : 1 1 0)



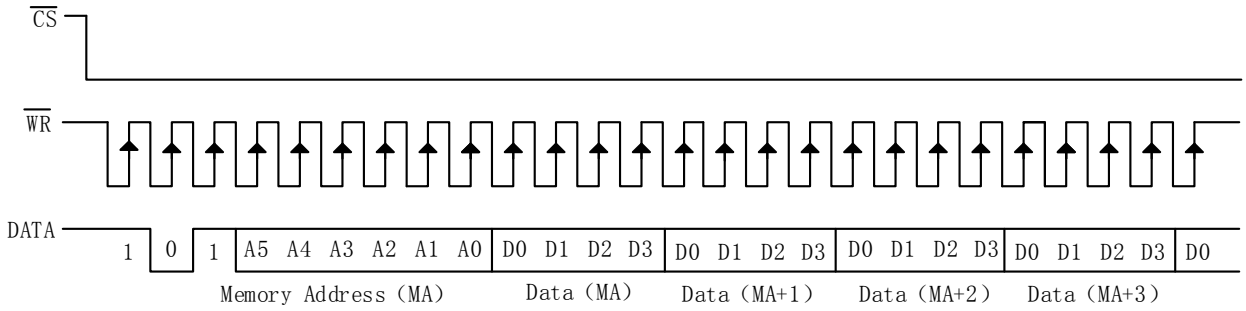
b. READ Mode (Successive Address Reading)



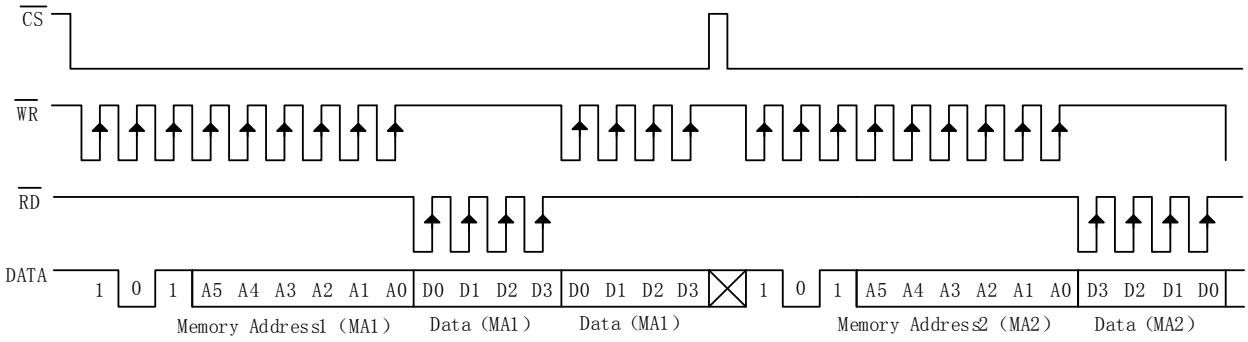
c. WRITE Mode (Command Code : 1 0 1)



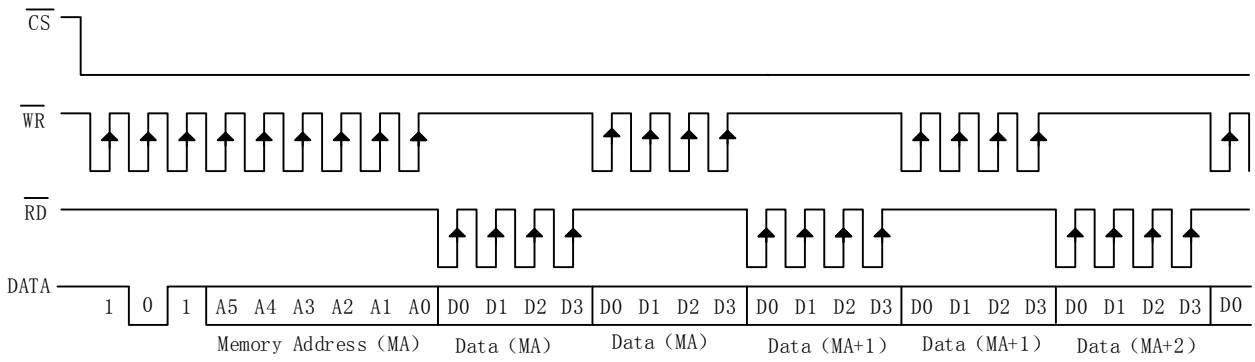
d. WRITE Mode (Successive Address Writing)



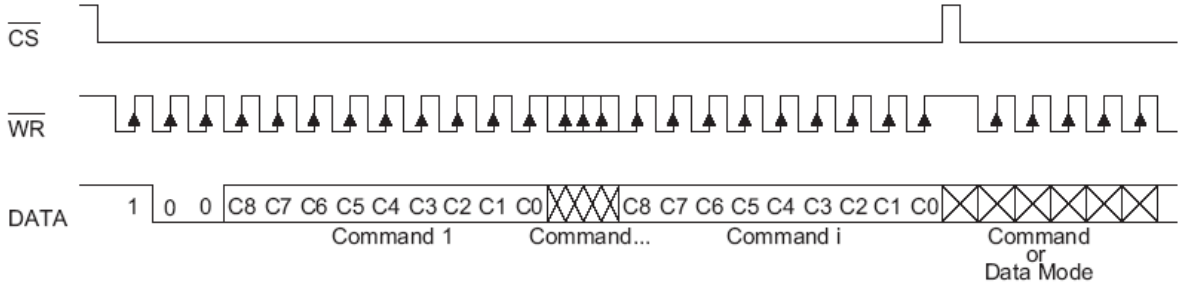
e. Read-Modify-Write Mode (Command Code : 1 0 1)



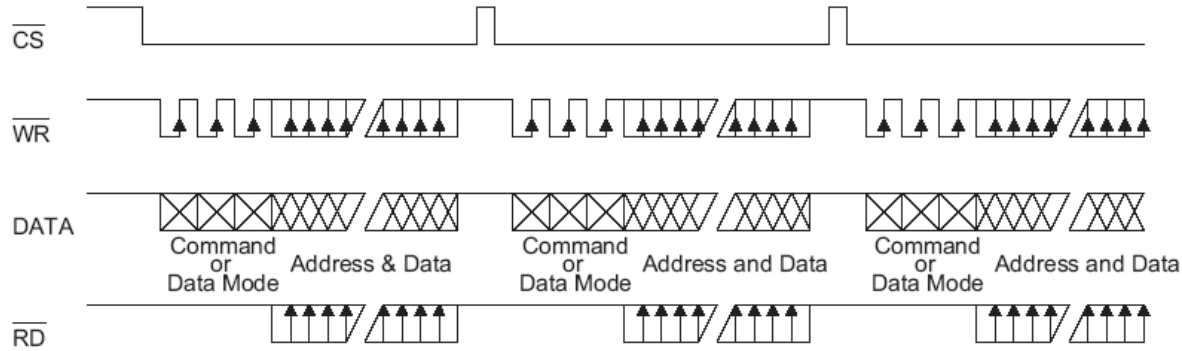
f. Read-Modify-Write Mode (Successive Address Accessing)



g. Command Mode (Command Code : 1 0 0)



h. Mode (Data And Command Mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

Command Summary

Name	ID	CommandCode	D/C	Function	Def.
READ	**110**	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**101**	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**101**	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**100**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes

SYS EN	**100**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**100**	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	**100**	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	**100**	0000-0100-X	C	Disable time base output	
WDT DIS	**100**	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	**100**	0000-0110-X	C	Enable time base output	
WDT EN	**100**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**100**	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	**100**	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	**100**	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	**100**	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	**100**	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	**100**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	**100**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**100**	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	**100**	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 2K	**100**	010X-XXXX-X	C	Tone frequency, 2kHz	
TONE 4K	**100**	011X-XXXX-X	C	Tone frequency, 4kHz	
$\overline{IRQ}$ DIS	**100**	100X-0XXX-X	C	Disable $\overline{IRQ}$ output	Yes
$\overline{IRQ}$ EN	**100**	100X-1XXX-X	C	Enable $\overline{IRQ}$ output	
F1	**100**	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	

F2	**100**	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	**100**	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	**100**	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	**100**	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	**100**	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	**100**	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	**100**	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	Yes
TEST	**100**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**100**	1110-0011-X	C	Normal mode	Yes

Note: X : Don,t care

A5~A0 : RAM addresses

D3~D0 : RAM data

D/C : Data/command mode

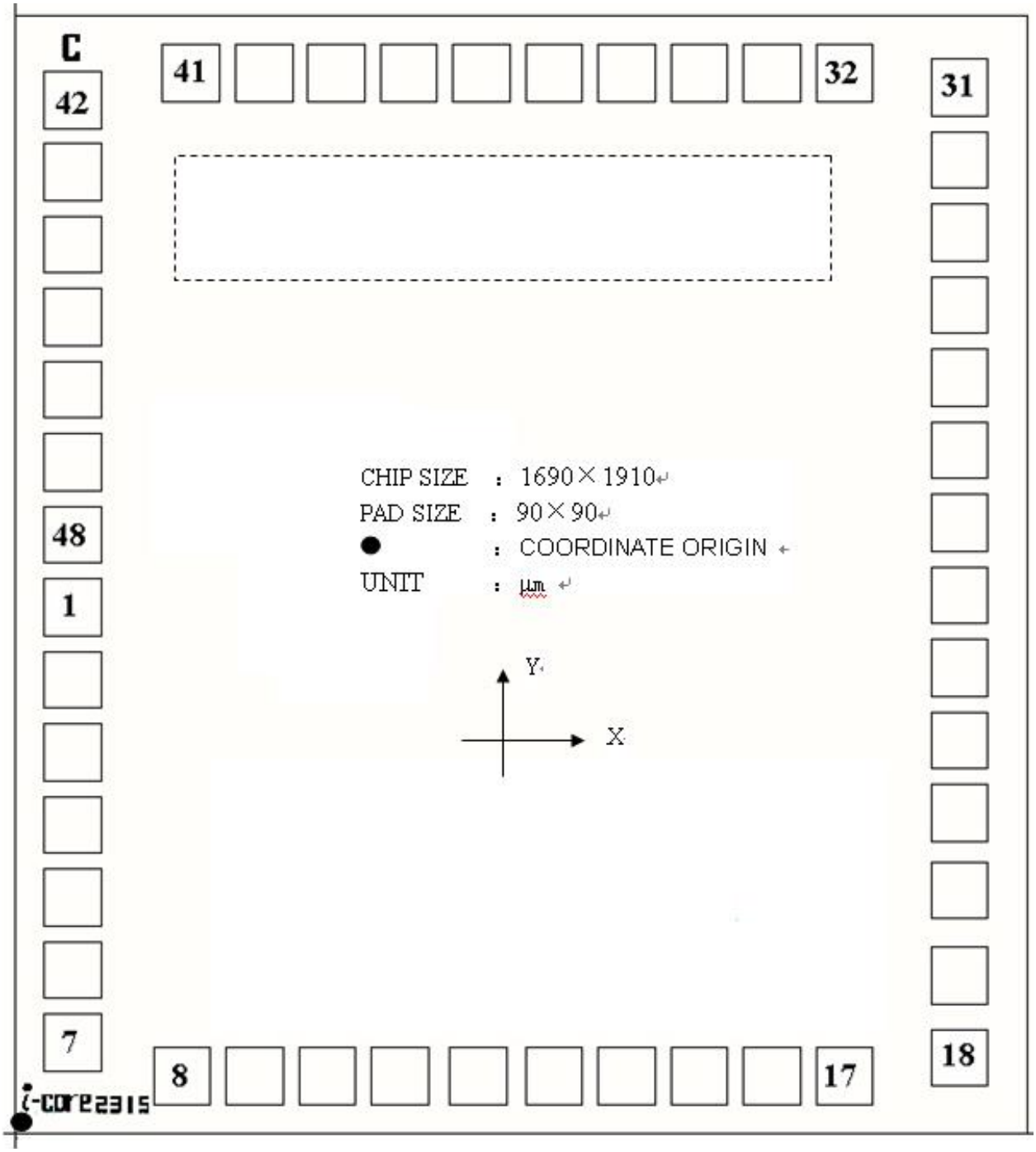
Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller

should initialize the CS1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the CS1621.

5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM



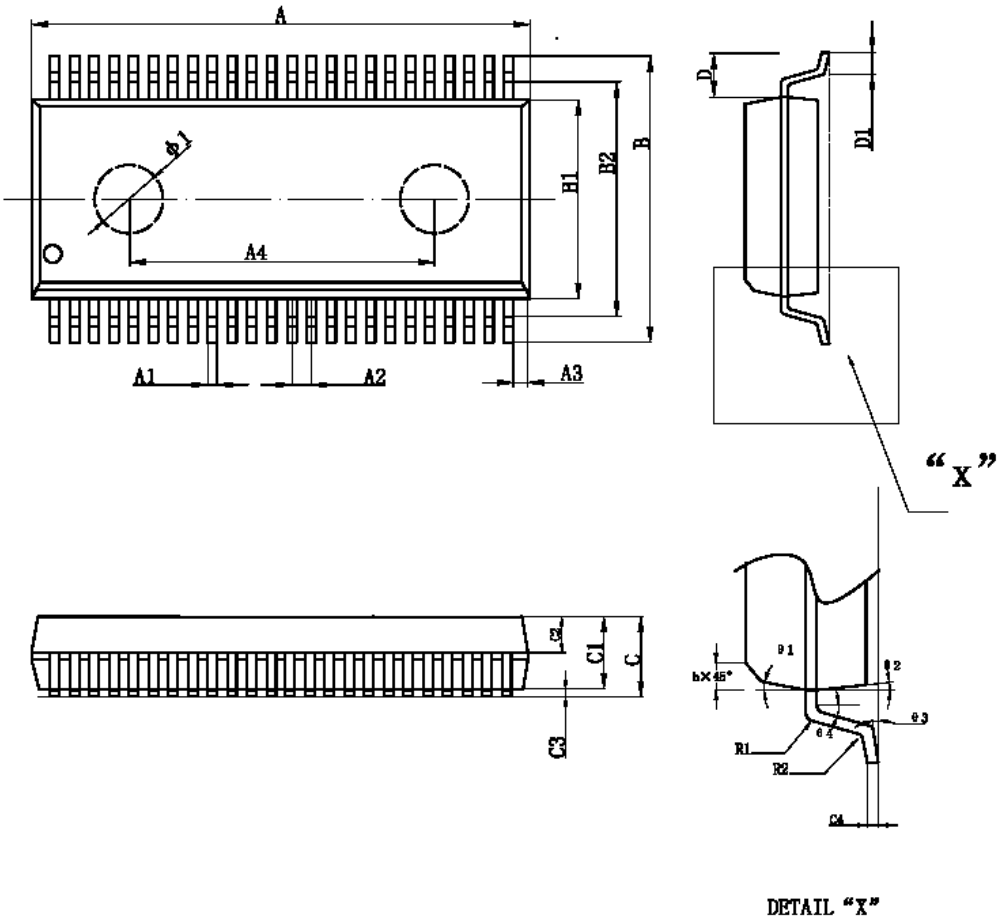
5.2、PAD Location （UNIT:μm）

PAD No.	PAD Name	(X, Y)	PAD No.	PAD Name	(X, Y)
1	SEG7	（46.10，789.15）	25	SEG31	（1451.75，923.55）
2	SEG6	（46.10，674.15）	26	SEG30	（1451.75，1038.55）
3	SEG5	（46.10，559.15）	27	SEG29	（1451.75，1153.55）
4	SEG4	（46.10，444.15）	28	SEG28	（1451.75，1268.55）
5	SEG3	（46.10，329.15）	29	SEG27	（1451.75，1383.55）
6	SEG2	（46.10，214.15）	30	SEG26	（1451.75，1498.55）
7	SEG1	（46.10，99.15）	31	SEG25	（1451.75，1613.55）
8	SEG0	（220.30，46.10）	32	SEG24	（1269.45，1636.10）
9	$\overline{CS}$	（335.30，46.10）	33	SEG23	（1154.45，1636.10）
10	$\overline{RD}$	（450.30，46.10）	34	SEG22	（1039.45，1636.10）
11	$\overline{WR}$	（565.30，46.10）	35	SEG21	（924.45，1636.10）
12	DATA	（689.45，46.10）	36	SEG20	（809.45，1636.10）
13	GND	（809.45，46.10）	37	SEG19	（694.45，1636.10）
14	OSCO	（924.45，46.10）	38	SEG18	（579.45，1636.10）
15	OSCI	（1039.45，46.10）	39	SEG17	（464.45，1636.10）
16	VLCD	（1154.45，46.10）	40	SEG16	（349.45，1636.10）
17	VDD	（1269.45，46.10）	41	SEG15	（234.45，1636.10）
18	$\overline{IRQ}$	（1451.75，75.25）	42	SEG14	（46.10，1594.15）
19	BZ	（1451.75，205.55）	43	SEG13	（46.10，1479.15）
20	BZN	（1451.75，339.95）	44	SEG12	（46.10，1364.15）
21	COM0	（1451.75，463.55）	45	SEG11	（46.10，1249.15）
22	COM1	（1451.75，578.55）	46	SEG10	（46.10，1134.15）
23	COM2	（1451.75，693.55）	47	SEG9	（46.10，1019.15）
24	COM3	（1451.75，808.55）	48	SEG8	（46.10，904.15）

6、PACKAGE INFORMATION

6. 1、 SSOP48

尺寸 / 标注	最 小（mm）	最 大（mm）	尺寸 / 标注	最 小（mm）	最 大（mm）
A	15. 77	15. 97	C3	0. 2	0. 4
A1	0. 20	0. 35	C4	0. 12	0. 25
A2	0. 635TYP		D	1. 41TYP	
A3	0. 5TYP		D1	0. 61	0. 91
A4	10. 2TYP		h	0. 381	0. 635
B	10. 01	10. 61	ϕ1	2. 2TYP	
B1	7. 39	7. 59	θ1	15° TYP	
B2	8. 6TYP		θ2	15° TYP	
C	2. 41	2. 78	θ3	4° TYP	
C1	2. 18	2. 38	θ4	8° TYP	
C2	1. 067TYP				



7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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