AIP31520

DOT MATRIX LCD DRIVER

1、GENERAL DESCRIPTION

The AIP31520 is a dot matrix LCD driver LSI intended for display of characters and graphics. The bit-addressable display data, which is sent from a microcomputer, is stored in a built-in display data RAM and generates the LCD drive signal.

The AIP31520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the AIP31520 permits the user to implement high-performance handy systems operating from a miniature battery.

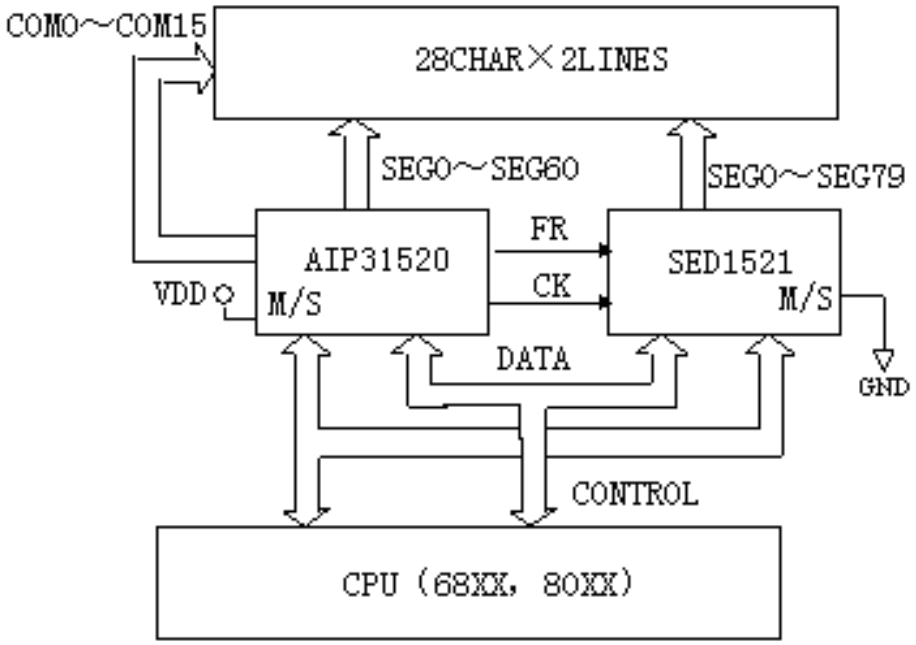
In order for the user to adaptively configure his system, the AIP31520 family offers two application forms. One form allows an LCD display of 12 characters 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

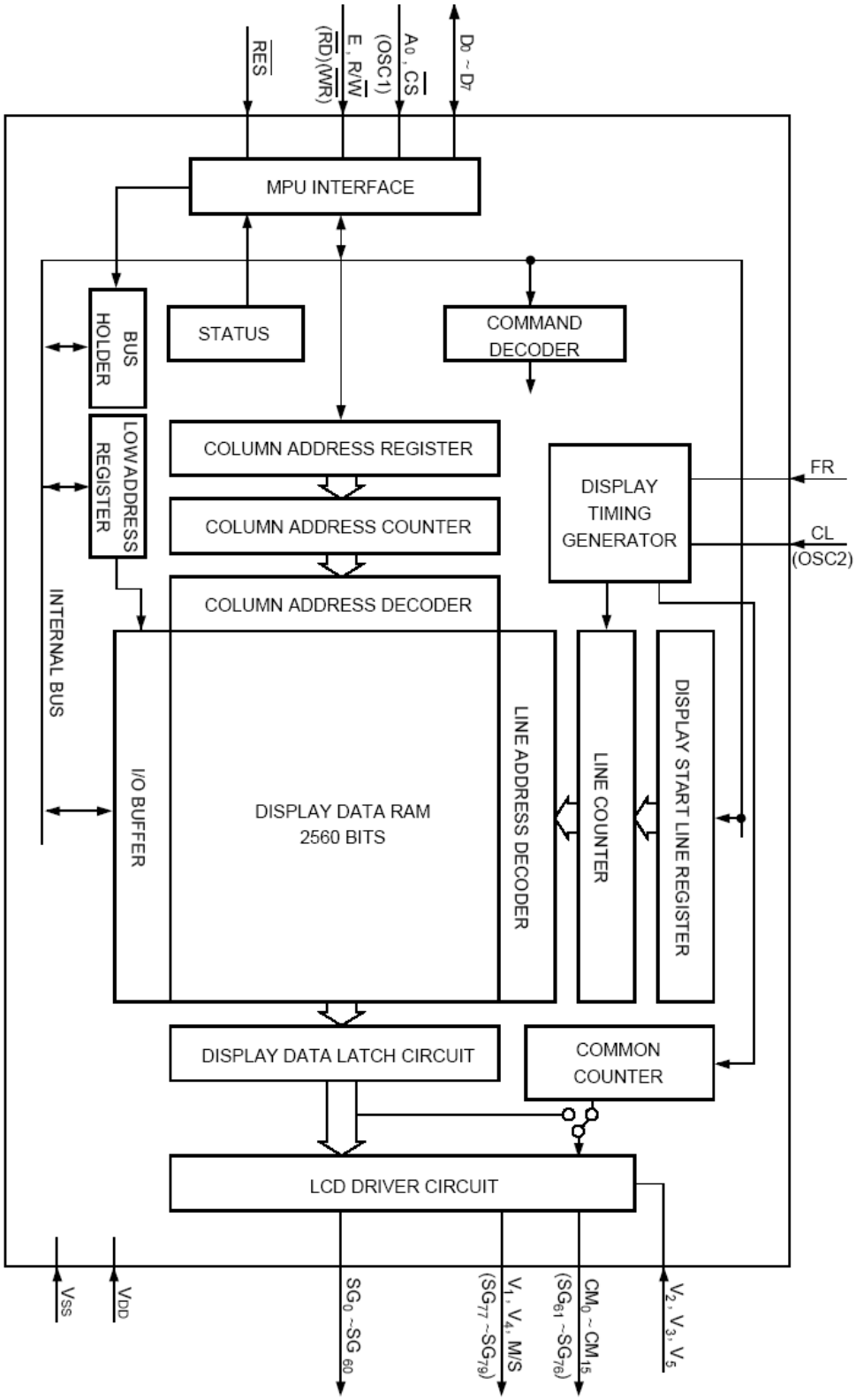
Features

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- Built-in display data RAM. . . 2560 bits
- Rich display command setting
- Master/slave operation is supported
- Low power consumption . . . 30μW
- LCD voltage . . . . . 3.5 to 13V
- Single power supply. . . . . 2.4 to 7.0V
- Chip size: 2670×3695 (μm×μm)
- The IC substrate should be connected to VDD or float in the PCB layout artwork.
- QFP100 or bare chip available

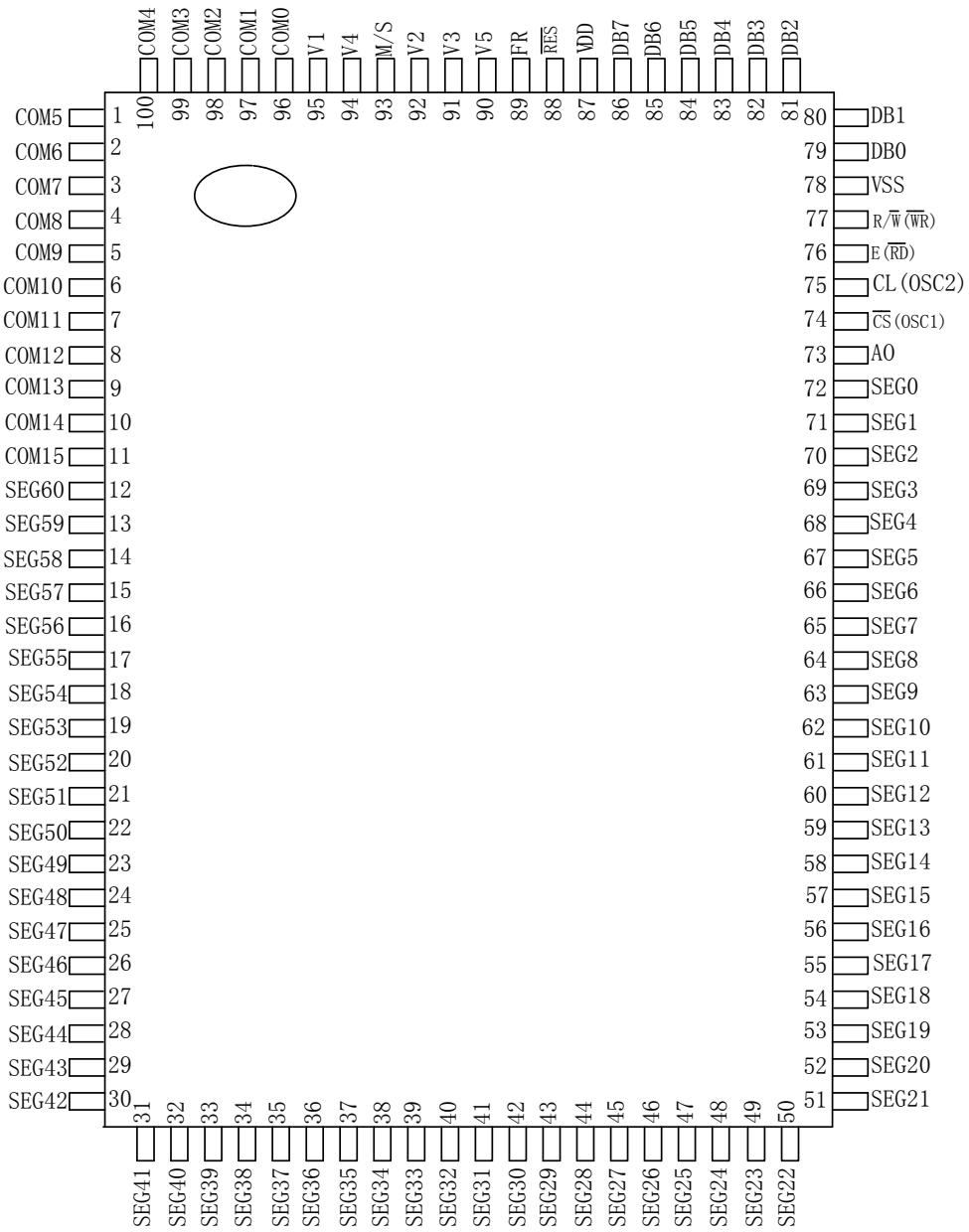
2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM




RES
E, R/W (RD)(WR)
(OSC1)
A0, CS
D0 ~ D7
MPU INTERFACE
BUS HOLDER
STATUS
COMMAND DECODER
LOW ADDRESS REGISTER
COLUMN ADDRESS REGISTER
COLUMN ADDRESS COUNTER
COLUMN ADDRESS DECODER
DISPLAY TIMING GENERATOR
FR
CL (OSC2)
INTERNAL BUS
I/O BUFFER
DISPLAY DATA RAM 2560 BITS
LINE ADDRESS DECODER
LINE COUNTER
DISPLAY START LINE REGISTER
DISPLAY DATA LATCH CIRCUIT
COMMON COUNTER
LCD DRIVER CIRCUIT
VSS
VDD
SG0 ~SG60
V1, V4, M/S (SG77 ~SG79)
CM0 ~CM15 (SG61 ~SG76)
V2, V3, V5

2.2、PIN CONFIGURATIONS



2.3、PIN DESCRIPTION

Pin No.	Pin Name	Description
87	VDD	Connected to +5V power. Common to MPU power pin VCC.
78	VSS	0V, connected to system GND.
95~94 90~92	V1～V5	Multi-level power used to drive LCDs. Voltage specified to each LCD cell is divided by resistors or impedance-converted by an operational amplifier before being applied. Each voltage to be applied must be based on VDD, while fulfilling the following conditions: VDD≥V1≥V2 ≥V3≥V4≥V5
79~86	D7～D0	8–bit, tri-state, bi-directional I/O bus. Normally, connected to the data bus of an 8–/16–bit standard microcomputer.
73	A0	Input pin. Normally, the LSB of the MPU address bus is connected to this input pin to provide data/command selection. 0: Display control data on D7–D0 1: Display data on D7–D0
88	$\overline{RES}$	Input pin. The AIP31520 can be reset or initialized by setting RES to low level (if it is interfaced with a 68 family MPU) or high level (if with an 80 family MPU). This reset operation occurs when an edge of the RES signal is sensed. The level input selects the type of interface with the 68 or 80 family MPU: High level: Interface with 68 family MPU Low level: Interface with 80 family MPU
74	$\overline{CS}$ (osc1)	Chip Select input signal which is normally obtained by decoding an address bus signal. Effective with “L” active and a chip operating with external clocks. For a chip containing an oscillator, $\overline{CS}$ works as an oscillation amplifier input pin to which an oscillation resistor (Rf) is connected. In this case, $\overline{RD}$, $\overline{WR}$ and E must be a signal ANDed with CS.
76	E（$\overline{RD}$）	Chip interfaced with 68 family MPU: Enable Clock signal input for the 68 family MPU. Chip interfaced with 80 family MPU: “L” Active input pin to which the 80 family MPU $\overline{RD}$ signal is connected. With this signal held at “L”, the AIP31520 data bus works as output.
77	R/W （$\overline{WR}$）	Chip interface with 68 family MPU: Read/Write control signal input pin. R/W = “H” : Read R/W = “L” : Write Chip interfaced with 80 family MPU: “L” Active input pin to which the 80 family $\overline{WR}$ is connected. The signal on the data bus is fetched by the leading edge of $\overline{WR}$.

<table>
<tr><td>75</td><td>CL(osc2)</td><td>Input signal effective with a chip using external clocks. This display data latch signal increments the line counter (at the trailing edge) or the common counter (at the leading edge). CL is connected to CL2 of the common driver. For a chip containing an oscillator, this pin works as the oscillation amplifier output pin to which an oscillation resistor (Rf) is connected.</td></tr>
<tr><td>89</td><td>FR</td><td>LCD AC signal I/O pin. Connected to pin M of the common driver.
I/O selection:
Chip containing commons M/S = 1 : Output
M/S = 0 : Input
Chip containing segments alone : Input</td></tr>
<tr><td>12~72</td><td>SEG0～
SEG60</td><td>LCD column (segment) driving output. One of the VDD, V2, V3 and V5 levels is selected by a combination of the content of display RAM and the FR signal. Fig 1</td></tr>
<tr><td>96~100
1~11</td><td>COM0～
COM15</td><td>LCD common (row) driving output. One of the VDD, V1, V4 and V5 levels is selected by a combination of the output of the common counter and the FR. Fig 2</td></tr>
<tr><td>93</td><td>M/S</td><td>Input signal which selects the master or slave LSI. Connected to VDD or VSS.
M/S = VDD: Master
M/S = VSS : Slave
M/S selection changes the function of pins FR, COM0–COM15, OSC1 (CS) and OSC2 (CL):
<table>
<tr><th>M/S</th><th>FR</th><th>COM output</th><th>OSC1</th><th>OSC2</th></tr>
<tr><td>VDD</td><td>Output</td><td>COM0～
COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>VSS</td><td>Input</td><td>COM31～
COM16</td><td>NC</td><td>Input</td></tr>
</table>
</td></tr>
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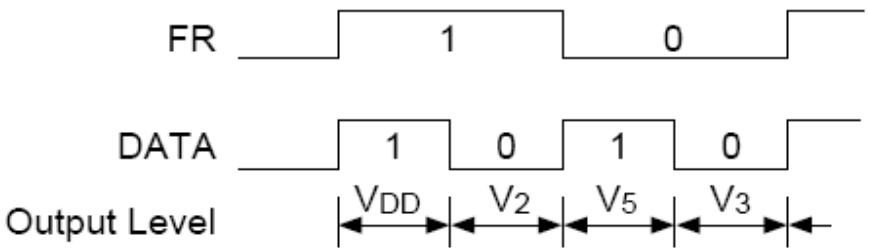


Fig.1 LCD Column (Segment) Driving Output Timing

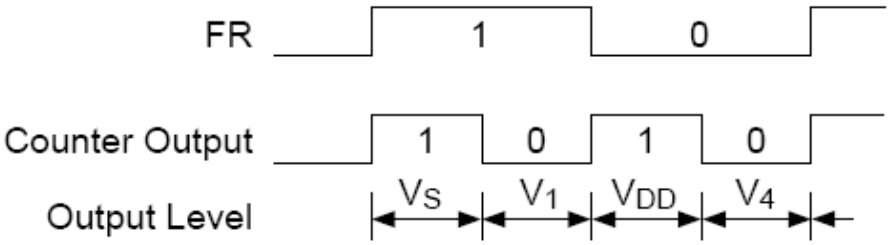


Fig.2 LCD Common (row) driving output

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Value	Unit
Supply voltage (1)	VSS		-8～+ 0.3	V
Supply voltage (2)	V5		-16.5～+0.3	V
Supply voltage (3)	V1、V2、V3、V4		V5～+0.3	V
Input voltage	V_{IN}		VSS-0.3～+0.3	V
Output voltage	V_{OUT}		VSS-0.3～+0.3	V
Allowable loss	P_D		250	mW
Operating temperature	T_{OPR}		-30～+85	℃
Storage temperature	T_{STG}		-65～+150	℃
Soldering temperature	T_{SOLDER}	10s	245	℃

Notes:

1. All voltages are based on VDD = 0V.
2. The following condition must always hold true with voltages V1, V2, V3, V4 and V5:
   VDD≥ V1≥ V2 ≥V3≥V4 ≥V5
3. The LSI may be permanently damaged if used with any value in excess of the absolute maximum ratings. During normal operation, the LSI should preferably be used within the specified electrical characteristics. Failure to meet them can cause the LSI to malfunction or lose its reliability.
4. Generally, flat package LSIs may have moisture resistance lowered when solder dipped. In mounting LSIs on a board, it is recommended to use a method which is least unlikely to give thermal stress on the package resin.

3.2、ELECTRICAL CHARACTERISTICS

(Tamb=25°C , VDD=2.5V, fosc=3.579545MHz, unless otherwise specified)

3.2.1 DC Characteristics (VDD=0V,Ta=-20～75℃)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)*1	Recommended	VSS		-5.5	-5.0	-4.5	V	VSS
	Allowable			-7.0		-2.4		
Operating Voltage （2）	Recommended	V5		-13.0		-3.5	V	V5 *10
	Allowable			-13.0				
	Allowabl	V1，V2		0.6×V5		VDD	V	V1，V2
	Allowable	V3，V4		V5		0.4×V5	V	V3，V4
High level input voltage		VIHT		VSS+2.0		VDD	V	*2 *3
		VIHC		0.2×VSS		VDD		
Low level input voltage		VILT		VSS		VSS+0.8	V	*2 *3
		VILC		VSS		0.8×VSS		
High level output voltage		VOHT	IOH=-3.0mA	VSS+2.4			V	*4 *5 OSC2
		VOHC1	IOH=-2.0mA	VSS+2.4				
		VOHC2	IOH=-120uA	0.2×VSS				
Low level output voltage		VOLT	IOL=3.0mA			VSS+0.4	V	*4 *5 OSC2
		VOLC1	IOL=2.0mA			VSS+0.4		
		VOLC2	IOL=120uA			0.8×VSS		
Input leakage current		ILI		-1.0		1.0	uA	*6
Output leakage current		ILO		-3.0		3.0	uA	*7
LCD driver ON resistor		RON	Ta=25℃ V5=-5.0V		5.0	7.5	KΩ	SEG0～60*11 COM0～15
			Ta=25℃ V5=-3.5V		10.0	50.0		
Static current dissipation		IDDQ	$\overline{CS}$ =CL=VDD		0.05	1.0	uA	VDD
Dynamic current dissipation		IDD(1)	V5=-5.0V fCL=2KHz		2.0	5.0	uA	VDD *12 *13 *14
			V5=-5.0V Rf=1MΩ		9.5	15.0		
			V5=-5.0V fCL=18KHz		5.0	10.0		
		IDD(2)	tcyc==200KHz		300	500	uA	*8
Input pin capacitance		CIN	Ta=25℃ f=1MHz		5.0	8.0	pF	All input pins
Oscillation frequency		fOSC	Rf=1.0MΩ±2% VSS=-5.0V	15	18	21	KHz	*9
			Rf=1.0 MΩ±2% VSS=-3.0V	11	16	21		
Reset time		tR		1.0		1000	us	$\overline{RES}$

Note: *1. Operation over a wide range of voltages is guaranteed except where a sudden voltage change occurs during access.

*2.Pins A0,D0 ~ D7,E（$\overline{RD}$）,R/W（$\overline{WR}$）and $\overline{CS}$.

*3. Pins CL,FR,M/S and $\overline{RES}$

*4. Pins D0 ~ D7

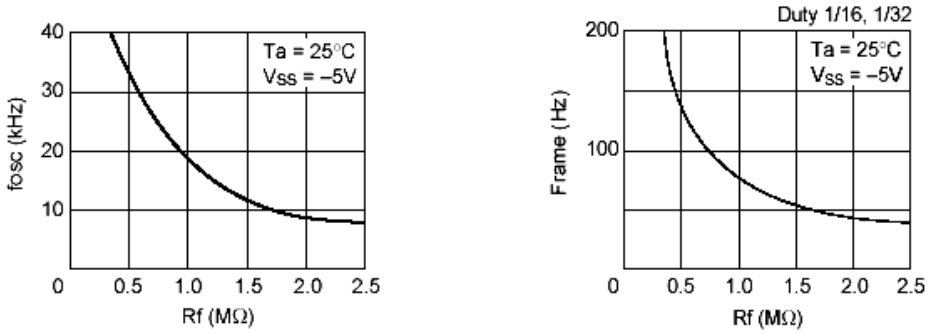
*5. Pins FR

*6. Pins A0, E（$\overline{RD}$）,R/W（$\overline{WR}$）,$\overline{CS}$,CL and $\overline{RES}$

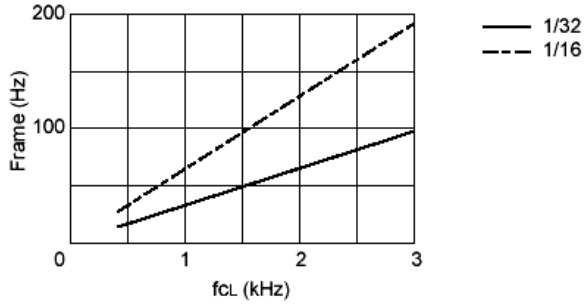
*7. Applicable when pins D0–D7 and FR are at high impedance.

*8. This value is current consumption when a vertical stripe pattern is written at tCYC. Current consumption during access is nearly proportionate to access frequency (tCYC). Only TDD (1) is consumed while no access is made.

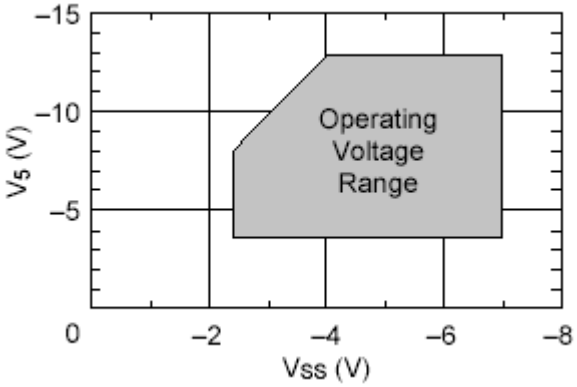
*9. Relationship between oscillation frequency, frame and Rf



Relationship between external clock (fCL) and frame (SED1520FAA)



*10.Operating voltage ranges of VSS and V5



*11.Resistance with a voltage of 0.1V applied between the output pin (SEG, COM) and each power pin (V1, V2, V3, V4). It is specified within the operating voltage range.

*12, 13, 14. Current consumed by each discrete IC, not including LCD panel and wiring capacitances.

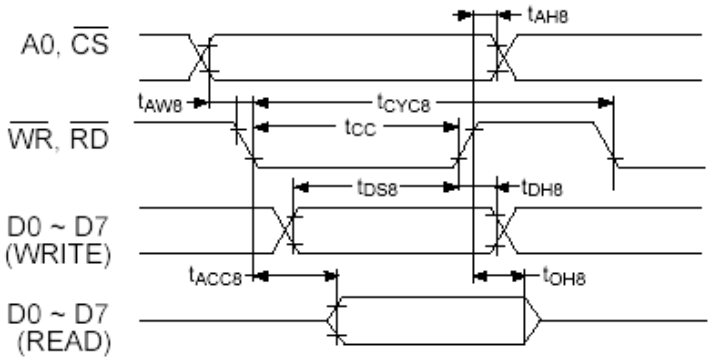
*12. Applicable to AIP31520 and SED1521FAA

*13. Applicable AIP31520

*14. Applicable SED1521FOA

3.2.2 AC Characteristics

- **System Bus Read/Write I (80 Family MPU)**



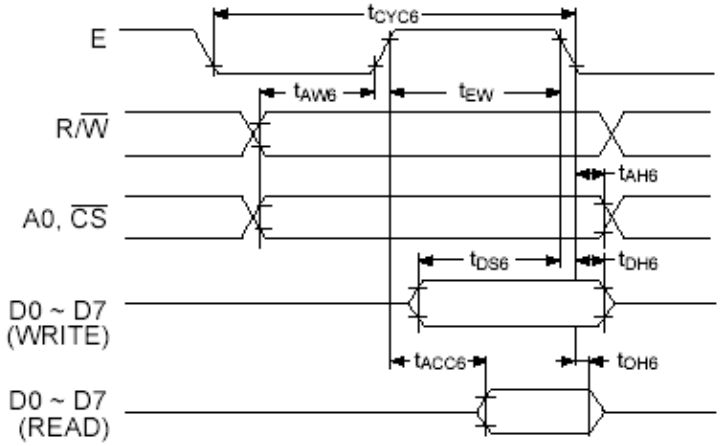
Ta=-20～75℃,VSS=-5.0V±10%

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0，$\overline{CS}$	tAH8		10		ns
Address setup time		tAW8		20		
System cycle time	$\overline{WR}$,$\overline{RD}$,	tcyc8		1000		ns
Control pulse width		tcc		200		
Data setup time	D0～D7	tDS8		80		ns
Data hold time		tDH8		10		
$\overline{RD}$ access time		tACC8	CL=100pF		90	
Output disable time		tOH8		10	60	

*1. Each of the values where VSS = –3.0V is about 200% of that where VSS = –5.0V

*2. The rise or fall time of input signals should be less than 15 ns.

● System Bus Read/Write II (68 Family MPU)



Ta=-20～75℃,VSS=-5.0V±10%

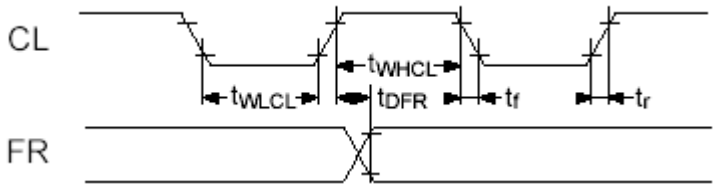
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time Address setup time Address hold time		A0，$\overline{CS}$ R/$\overline{W}$	tyc6 *1 tAW6 tAH8		1000 20 10		ns
Data setup time Data hold time Output disable time Access time		D0～D7	tDS6 tDH6 tOH6 tACC6	 CL=100pF 	80 10 10 	 60 90	ns
Enable pulse width	Read	E	tEW		100		ns
	Write				80		ns

*1. tCYC6 indicates the cycle time during which CS•E = “H”. It does not mean the cycle time of signal E.

*2. Each of the values where VSS = –3.0V is about 200% of that where VSS = –5.0V

*3. The rise or fall time of input signals should be less than 15 ns.

● Display Control Timing



● Input Timing

Ta=-20～75℃,VSS=-5.0V±10%

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	tWLCL		35			us
High level pulse width		tWHCL		35			us
Rise time		tr			30	150	ns
Fall time		tf			30	150	ns
FR delay time	FR	tDFR		-2.0	0.2	2.0	us

● Output Timing

Ta=-20～75℃,VSS=-5.0V±10%

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	tDFR	CL=100pF		0.2	0.4	us

*1. The listed FR input delay time applies to the SED1521 and AIP31520 (slave).
The listed FR output delay time applies to the AIP31520 (master).
*2. Each of the values where VSS = –3.0V is about 200% of that where VSS = –5.0V.

4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

APPLICATION NOTE

MPU Interface

● Selection of Interface Type

The AIP31520 Series uses 8 bits of bi-directional data bus (D0–D7) to transfer data. The reset pin is capable of selecting MPU interface; setting the polarity of RES to either “H” or “L” can provide direct interface of the AIP31520 with a 68 or 80 family MPU (see Table 1 below).

Table 1:

Polarity of RES	Type	A0	E	R/W	CS	D0～D7
L	68 MPU	↑	↑	↑	↑	↑
H	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

- **Identification of Data Bus Signals**

The AIP31520 uses a combination of A0, E, R/W, (RD, WR) to identify a data bus signal.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

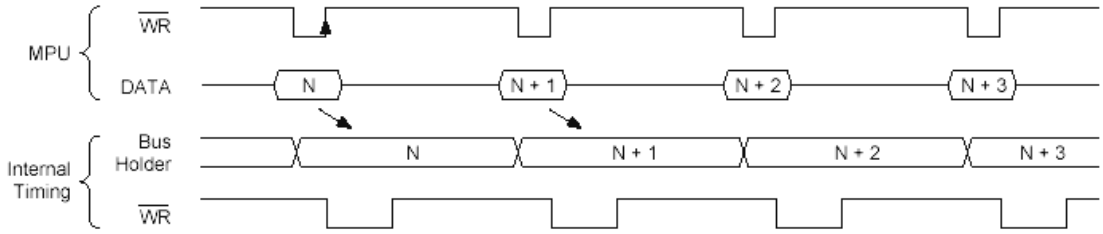
- **Access to Display Data RAM and Internal Register**

In order to make matching of operating frequencies between the MPU and the display data RAM or internal register, the AIP31520 performs a sort of LSI–LSI pipelining via the bus holder attached to the internal data bus.

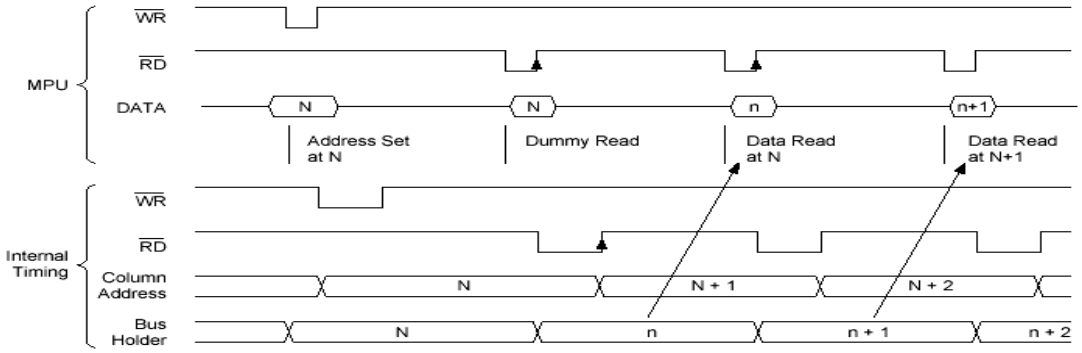
Consider the case where the MPU reads the content of the display data RAM. In the first data read cycle (dummy), the data is stored on the bus holder. In the next data read cycle, the data is read from the bus holder to the system bus.

Also, consider the case where the MPU writes data to the display data RAM. In the first data write cycle, the data is held on the bus holder. The data is written to the display data RAM before the next data write cycle begins.

a) Write Timing Diagram



b) Read Timing Diagram



- **Busy Flag**

Busy flag being “1” means that the AIP31520 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin D7 by a Read Status instruction. As long as the cycle time (t_{CYC}) requirement is met, the flag need not be checked before each command and this dramatically improves the MPU performance.

- **Display Start Line Register**

This register is a pointer which determines the start line corresponding to COM0 (normally, the uppermost line of display) for display of data in the display data RAM. It is used for scrolling the display or changing the page from one to another. Executing the Set Display Start Line command sets 5 bits of display start address in this register. Its content is preset in the line counter at each timing the FR signal changes. The line counter is incremented synchronously to a CL input, thus generating a line address for sequential reading of 80 bits of data from the display data RAM to the LCD driver circuit.

- **Column Address Counter**

The column address counter is a 7–bit presettable counter which gives column addresses of the display data RAM as shown in Fig.4 2. When a Read/Write Display Data command comes in, the counter is incremented by 1. For any nonexisting address over 50H, the counter is locked and not incremented.

The column address counter is independent from the page register.

- **Page Register**

This register gives a page address of the display data RAM as shown in Fig. 42. The Set Page Address command permits the MPU to access a new page of the display data RAM.

- **Display Data RAM**

Dot data for display is stored in this RAM. Since the MPU and LCD driver circuit operate independently of each other, data can be changed asynchronously without adverse effect on the display.

One bit of the display data RAM is assigned to one bit of LCD:

LCD on = “1”

LCD off = “0”

The ADC command inverts the assignment relationship between a display data RAM column address and a segment output (see Fig.4).

- **Common Timing Generator**

This circuit generates common timing and frame (FR) signals from the basic clock (CL). The Select Duty command selects a duty of 1/16 or 1/32. The 1/32 duty is achieved by a two-chip (master and slave) configuration (common multi-chip system).

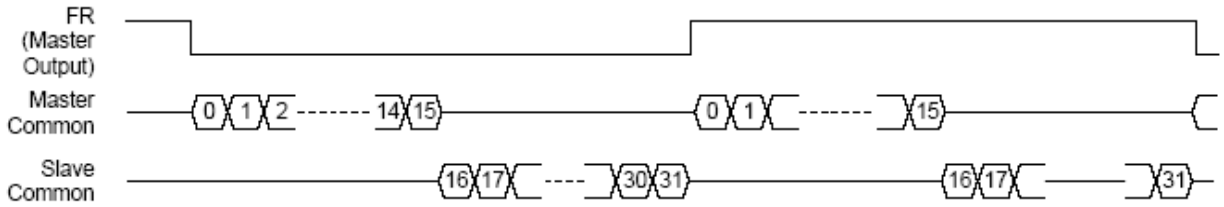


Fig.3 Common Timing Diagram

- **Display Data Latch Circuit**

The display data latch circuit temporarily stores the data which will be output from the display data RAM to the LCD driver circuit at one-common intervals. The display ON/OFF and Static Driver ON/OFF commands control the latched data so that the data in the display data RAM remains unchanged.

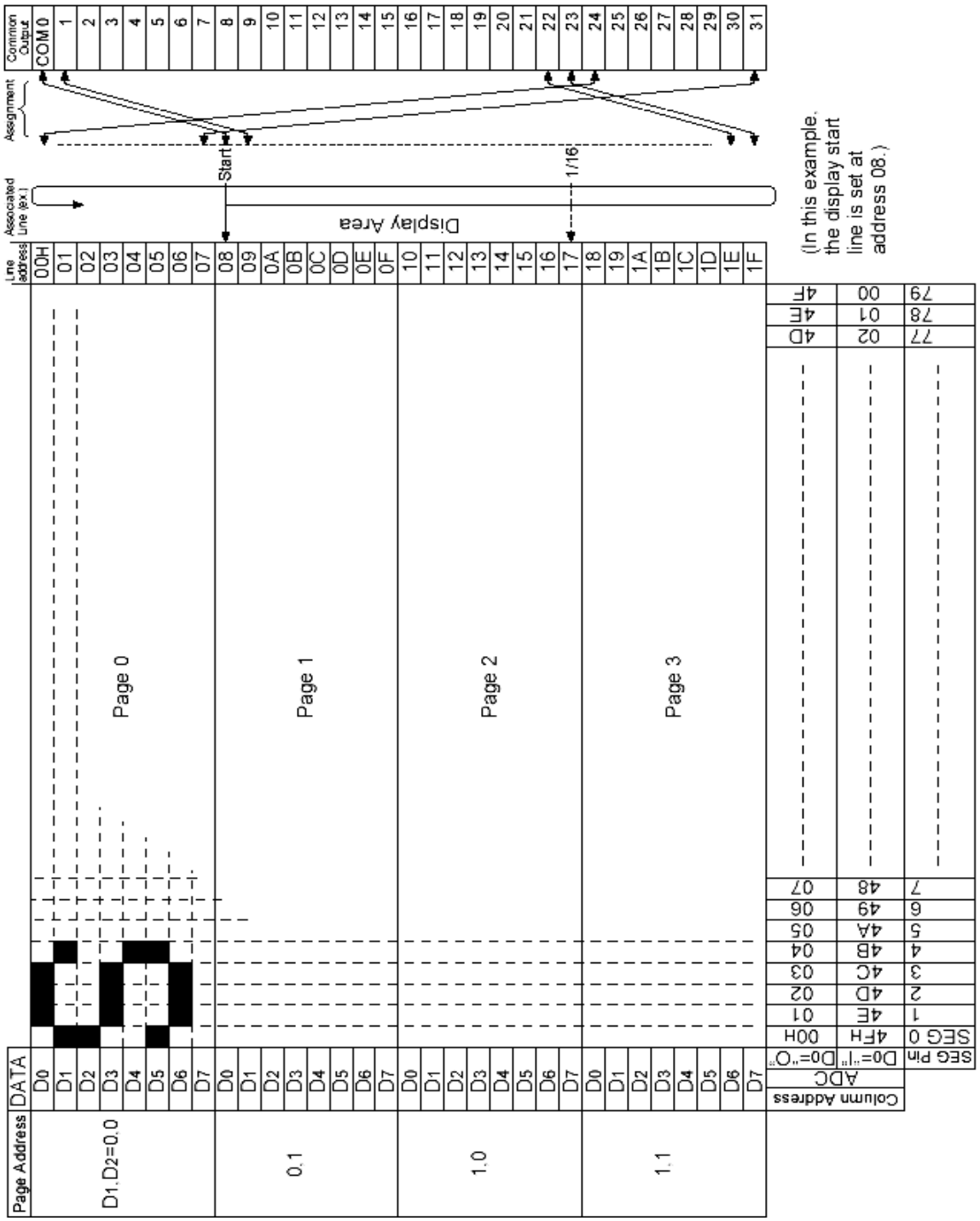


Fig.4 Relationship between Display Data RAM Locations and Addresses (Display Start Line: 08)

- **LCD Driver Circuit**

This circuit generates 80 sets of multiplexer that generate quartet levels for LCD driving. Display data in the display data latch, common timing generator output and FR signal are combined to output an LCD driving waveform

.

- **Display Timing Generator**

This circuit generates an internal display timing signal from the basic clock (CL) and frame signal (FR).

The frame signal FR makes the LCD driver circuit generate a dual frame AC driving waveform (type B) to drive LCD, while making both the line counter and common timing generator synchronized to the FR signal output LSI (dedicated common driver or the AIP31520 master LSI). To achieve these functions, the FR signal must be a clock with a duty of 50% which is synchronized to the frame period.

The clock CL is a clock used to operate the line counter. For a system in which both the AIP31520 and SED1521F coexist, they should be of LSI types having the same clock frequency to be applied to pin CL.

- **Oscillation Circuit**

This circuit is a low-power CR oscillator which uses an oscillation resistor Rf alone to adjust the oscillation frequency. It generates display timing signals. The AIP31520 is available in two LSI types if classified by oscillation: one LSI type contains an oscillation circuit and the other uses an externally provided clock.

The oscillation resistor Rf is connected as shown below. Where an LSI containing an oscillation circuit is operated with an external clock, it is necessary to input the clock with the same phase as OSC2 of the master LSI to OSC2 of the slave LSI.

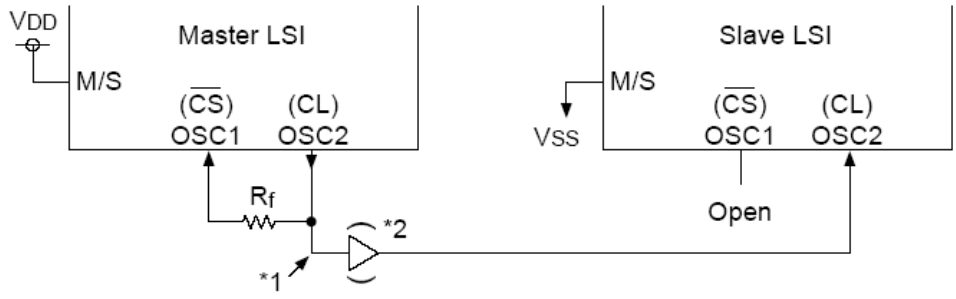


Fig. 5 LSIContaining Oscillator

NOTE: 1. As the parasitic capacitance in this portion increases, the oscillation frequency will shift to a lower level. The Rf musthave a smaller value than the specification.

2. For a system having two or more slave LSIs, a CMOS buffer is necessary.

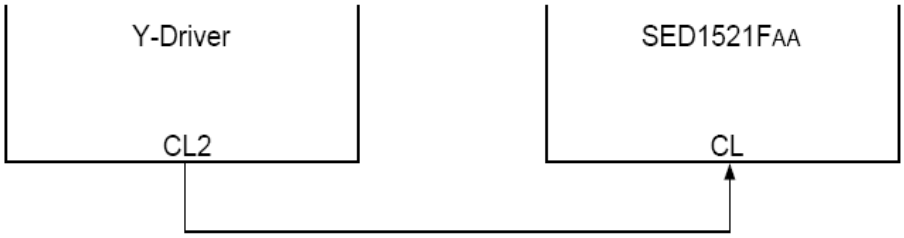


Fig.6 LSI Operating with External Clock

- **Reset Circuit**

This circuit senses the leading edge or trailing edge of $\overline{RES}$ and initializes the system when its power is switched on.

(a) Display off
(b) Display start line register: First line
(c) Static drive off
(d) Column address counter: Address 0
(e) Page address register: Page 0
(f) Select duty: 1/32
(g) Select ADC: Forward (ADC command D0 = “0”, ADC status flag = “1”)
(h) Read modify write off

The input at pin RES is level-sensed to select an MPU interface mode as shown in Table 1. For interfacing with an 80 family MPU, an “H” active reset signal is input to pin RES. For interfacing with a 68 family MPU, an “L” active reset signal is input to the pin.

As exemplified in section 6 “MPU Interface”, pin RES is connected to the MPU reset pin. Thus the AIP31520 and the MPU are initialized at the same time. If system is initialized by pin RES at power on, it may no longer be reset.

The Reset command causes initialization (b), (d) and (e).

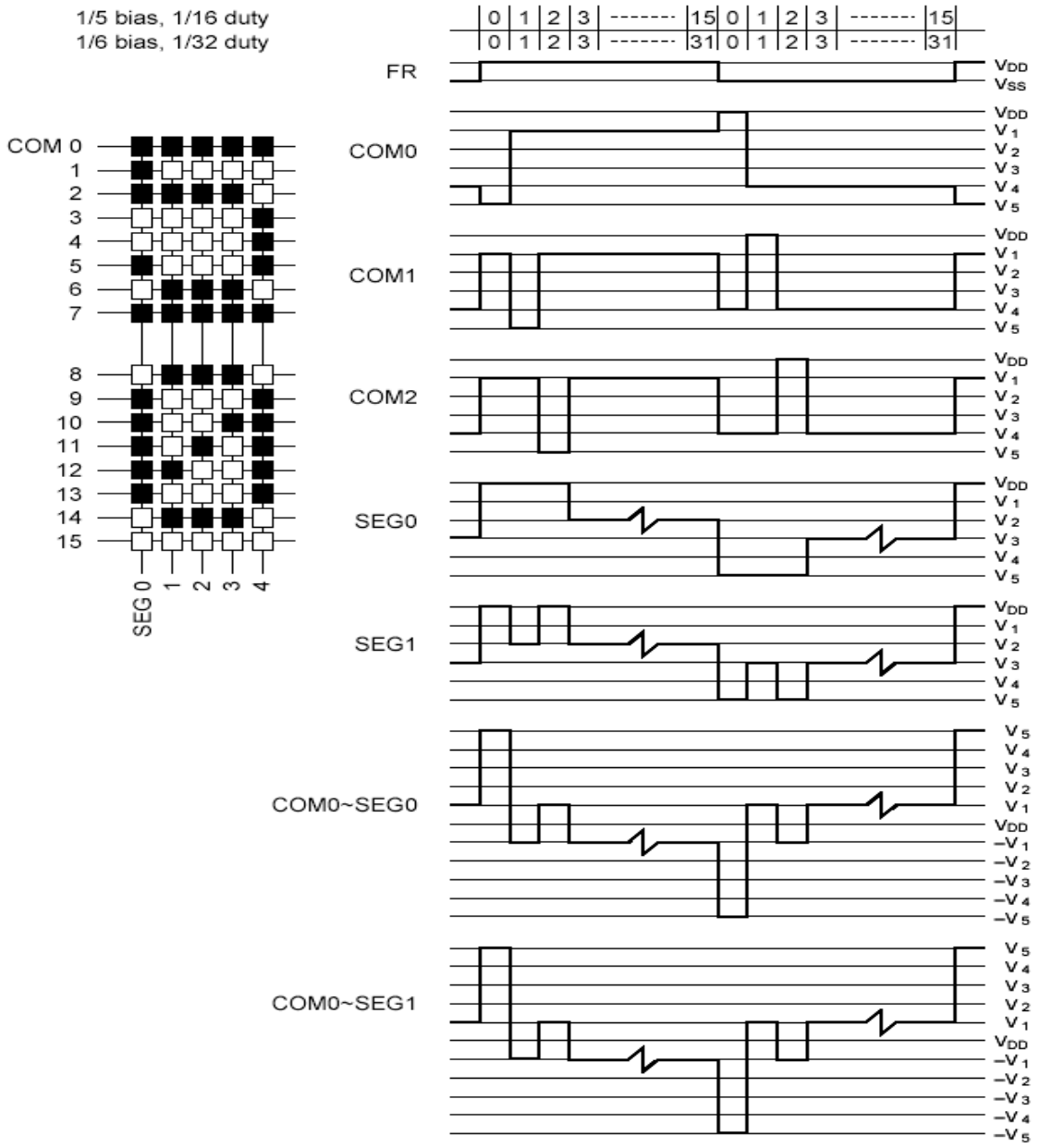


Fig. 7 Example of LCD Driving Waveform

Commands

Table 3 lists the commands used with the AIP31520. This LSI uses a combination of A0, R/W (RD, WR) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore, a command can be executed so fast that no busy check is needed.

Display ON/OFF

This command forces all display to turn on or off.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D =0: Display OFF
D =1: Display ON

Display Start Line

This command specifies a line address thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

A4 A3 A2 A1 A0	Line address
0 0 0 0 0	0
0 0 0 0 1	1
⋮	⋮
1 1 1 1 1	31

Set Page Address

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	0	A1	A0

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

Column Address

This command specifies a display data RAM column address. The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM. Thus, it is possible for the MPU to gain continuous access to only the data. This incrementing stops with address 80; the page address is not continuously changed.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

Read Status

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: BUSY being “1” means that system is performing an internal operation or is reset. No command is accepted before BUSY = “0”. As long as the cycle time requirement is met, no BUSY check is needed.

ADC: Indicates assignment of column addresses to segment drivers.

0: Inverted (column address 79-n ↔ segment driver n)

1: Forward (column address n ↔ segment driver n)

ON/OFF: Indicates display on or off.

0: Display on

1: Display off

This bit has polarity reverse to the Display ON/OFF command.

RESET: Indicates that system is being initialized by the REST signal or the Reset command.

0: Display mode

1: Being reset

Write Display Data

This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1; this enables the MPU to write multiword data continuously.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Read Display Data

This command allows the MPU to read 8 bits of data from the display data RAM location specified

by a column address and a page address. Once the data is read, the column address is automatically incremented by 1; this enables the MPU to read multi-word data continuously.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Select ADC

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software-invert the order of segment driver output pins, reducing the restrictions on the configuration of ICs at LCD module assembly.

D = 0: Clockwise output (forward)

D = 1: Counterclockwise output (reverse)

Static Drive ON/OFF

This command forces all display to be on and, at the same time, all common output to be selected.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D = 0: Static drive off

D = 1: Static drive on

Select Duty

This command is used to select the duty (degree of multiplexity) of LCD driving. It is valid for the AIP31520 (actively operating LSI) only, not valid for the SED1521F (passively operating LSI).The SED1521F operates with any duty determined by the FR signal.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

D = 0: Duty 1/16

D = 1: Duty 1/32

Read Modify Write

This command is used with the End command in a pair. Once it has been entered, the column address will be incremented not by the Read Display Data command but by the Write Display Data command only. This mode will stay until the End command is entered.

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area are repeatedly updated.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

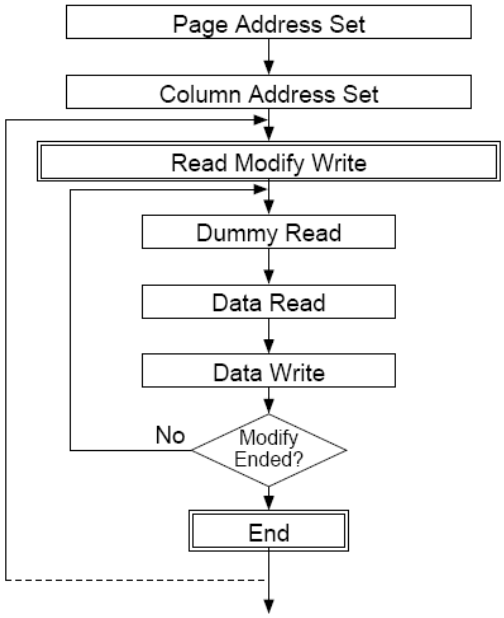


Fig.8 Cursor Blinking Sequence

END

This command cancels the Read Modify Write command, returning the column address to the initial mode address. See Fig8 and Fig.9

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

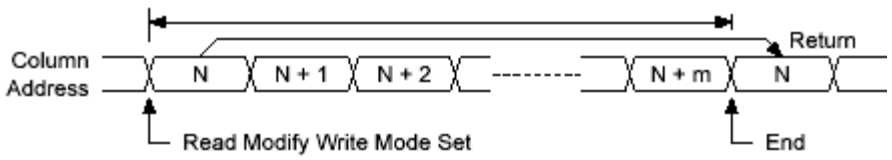


Fig.9.End Timing

RESET

This command initializes the display start line register, column address counter, and page address counter without any effect on the display data RAM.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Save Power(Combined Command)

Static drive going on with display off invokes power-saving mode, reducing current consumption to nearly static current level. During this mode, the AIP31520 holds the following conditions:

(a) It stops driving the LCD; the segment and common driver outputs are at VDD level.

(b) Oscillation and external clock input are disabled; OSC2 is in floating condition.

(c) The display data and operational mode are held.

The power-saving mode is cancelled by display on or static drive off.

If an external resistor division circuit is used to give LCD driving voltage level, the current flowing into the resistors must be cut off by the power-save signal.

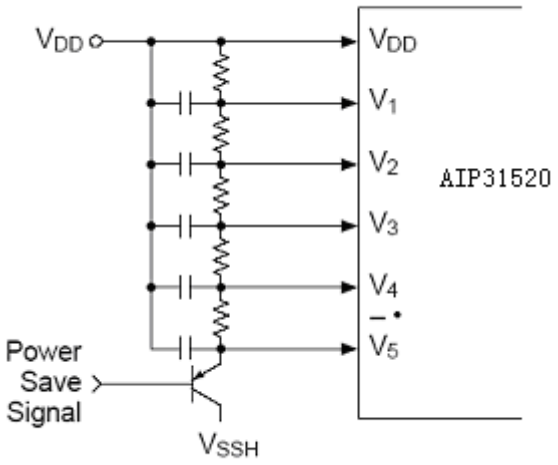


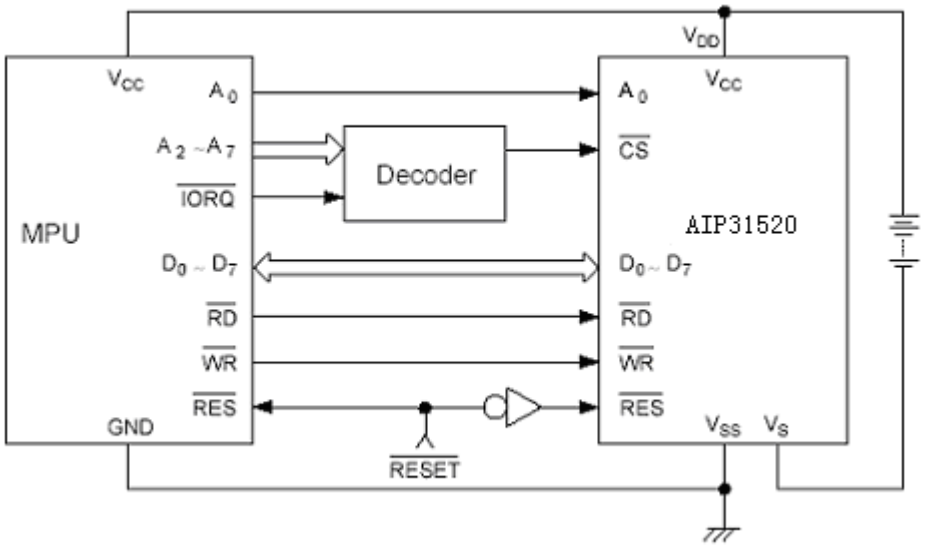
Fig.10.External Resistor Division Circuit

Table3 Command

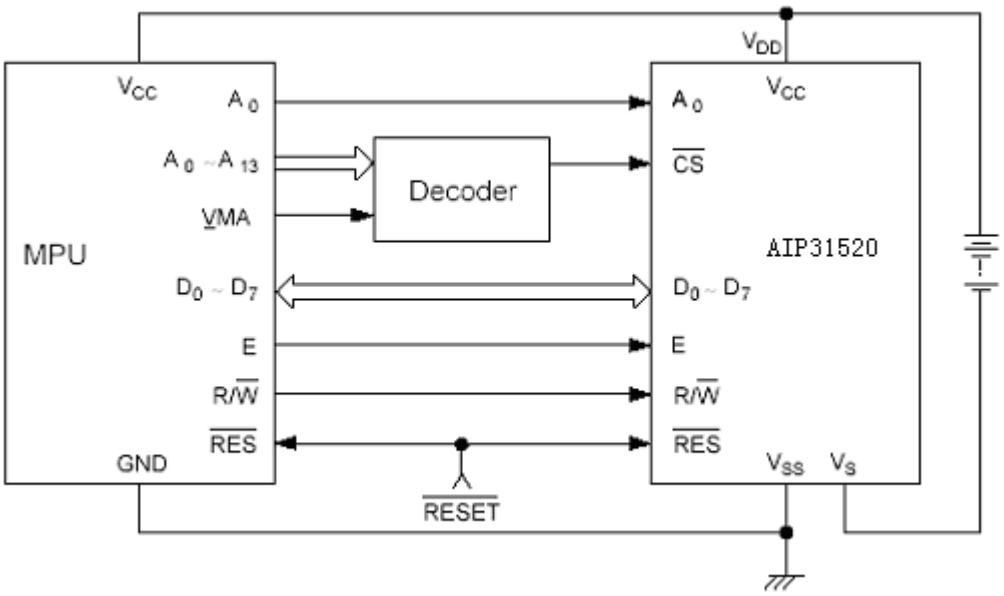
Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	1：ON 0：OFF
Display start line	0	1	0	1	1	0	Display Start Address （0～31）					Specifies RAM line corresponding to uppermost line (COM0) of display.

Set page address	0	1	0	1	0	1	1	1	0	Page（0～3）	Sets display RAM page in page address register.
Set column address	0	1	0	0	Column Address（0～79）						Sets display RAM column address in column address register.
Read status	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Internal operation, 0: Ready ADC 1: CW output (forward), 0: CCW output (reverse) ON/OFF 1: Display off, 0: Display on RESET 1: Being reset, 0: Normal
Write data	1	1	0	Write Data							Writes data from data bus into display RAM.
Read data	1	0	1	Read Data							Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output (forward) 1: CCW output (reverse)
Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	1：1/32 0：1/16
Read modify write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written.
END	0	1	0	1	1	1	0	1	1	1	0	Clears read modify write mode.
RESET	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.

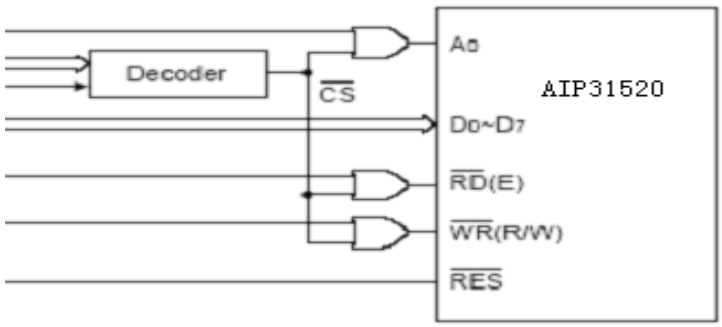
80 FAMILY MPU



68 FAMILY MPU

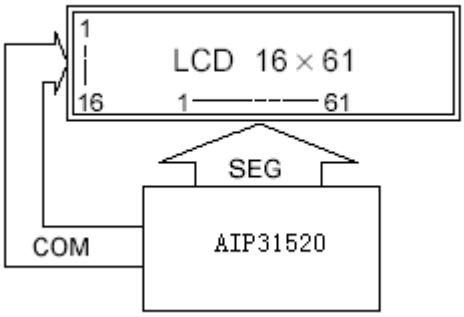


The AIP31520 (containing an oscillator) does not have pin CS. The output ORed with CS must be applied to pins A0, RD (E) and WR (R/W).

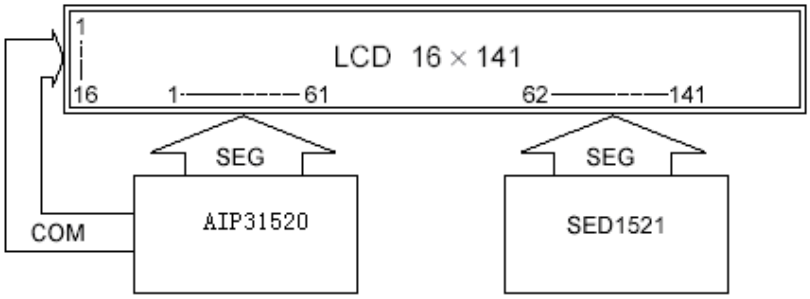


Typical Connections With LCD Panel

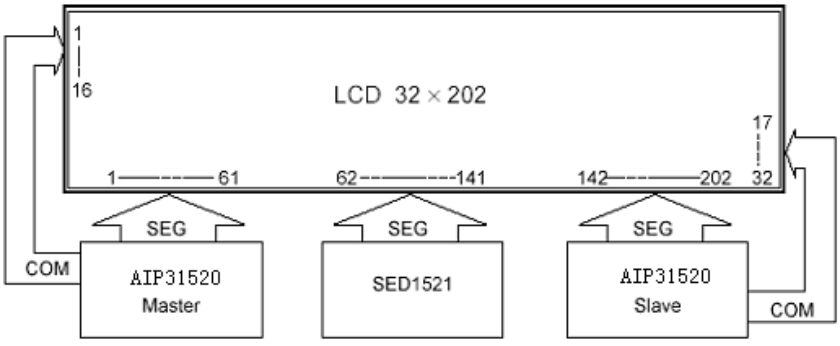
- Duty 1/16, 10 Characters X 2 Llines



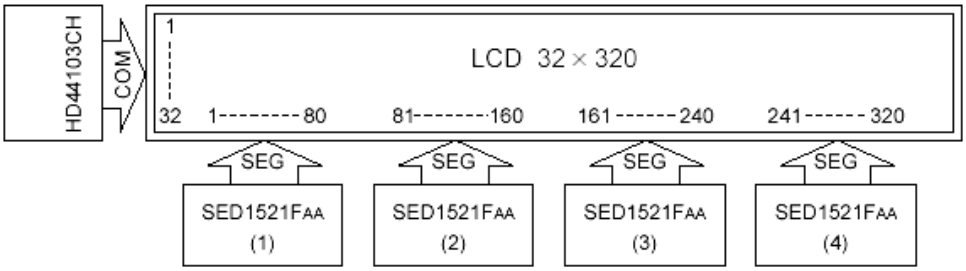
- **Duty 1/16, 23 Characters X 2 Lines**



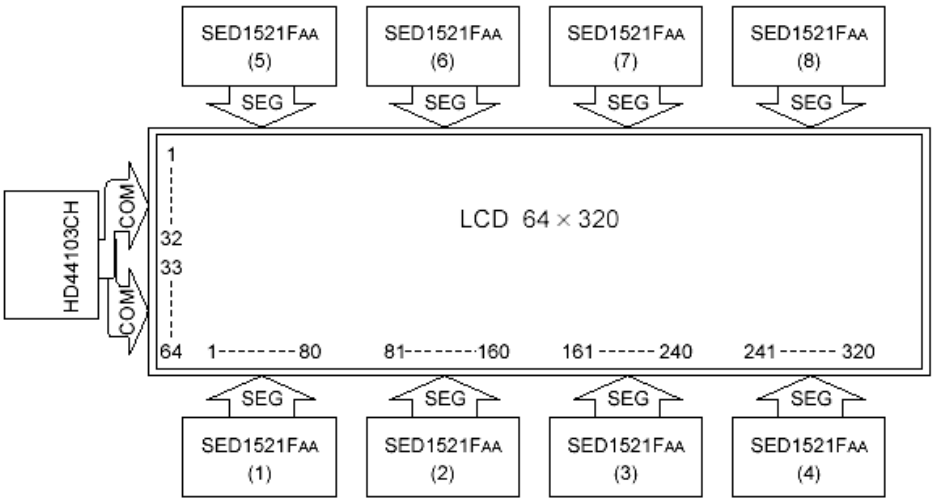
- **Duty 1/32, 33 Characters X 4 Lines**



- **Duty 1/32, 20 KANJI Characters X 2 Lines**

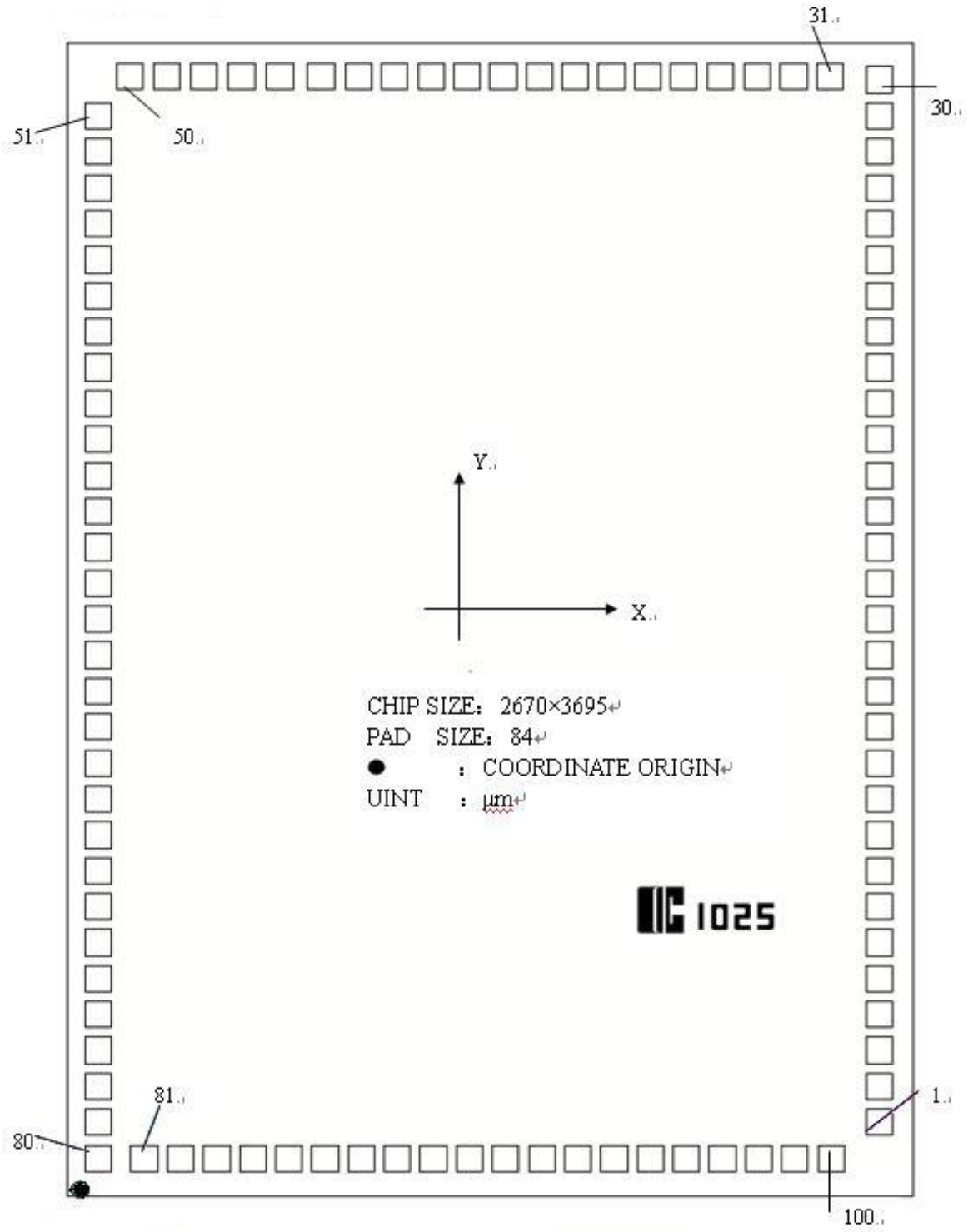


- **Duty 1/32, 2–Screen Display, 20 KANJI Characters X 4 Lines**



5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM

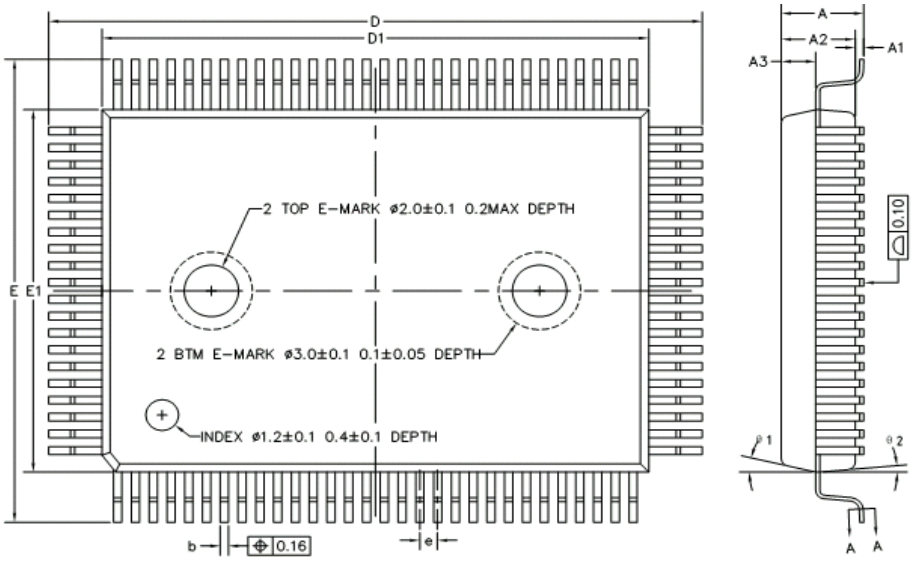


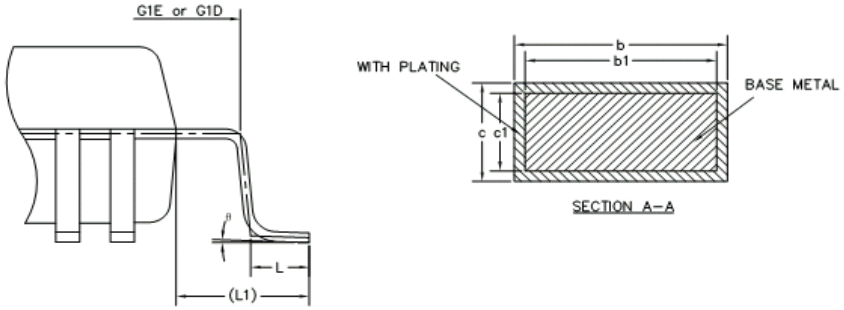
5.2、PAD Location （UNIT:μm）

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	COM5	2537.20	167.00	51	SEG21	52.00	3387.00
2	COM6	2537.20	282.00	52	SEG20	52.00	3272.00
3	COM7	2537.20	397.00	53	SEG19	52.00	3157.00
4	COM8	2537.20	512.00	54	SEG18	52.00	3042.00
5	COM9	2537.20	627.00	55	SEG17	52.00	2927.00
6	COM10	2537.20	742.00	56	SEG16	52.00	2812.00
7	COM11	2537.20	857.00	57	SEG15	52.00	2697.00
8	COM12	2537.20	972.00	58	SEG14	52.00	2582.00
9	COM13	2537.20	1087.00	59	SEG13	52.00	2467.00
10	COM14	2537.20	1202.00	60	SEG12	52.00	2352.00
11	COM15	2537.20	1317.00	61	SEG11	52.00	2237.00
12	SEG60	2537.20	1432.00	62	SEG10	52.00	2122.00
13	SEG59	2537.20	1547.00	63	SEG9	52.00	2007.00
14	SEG58	2537.20	1662.00	64	SEG8	52.00	1892.00
15	SEG57	2537.20	1777.00	65	SEG7	52.00	1777.00
16	SEG56	2537.20	1892.00	66	SEG6	52.00	1662.00
17	SEG55	2537.20	2007.00	67	SEG5	52.00	1547.00
18	SEG54	2537.20	2122.00	68	SEG4	52.00	1432.00
19	SEG53	2537.20	2237.00	69	SEG3	52.00	1317.00
20	SEG52	2537.20	2352.00	70	SEG2	52.00	1202.00
21	SEG51	2537.20	2467.00	71	SEG1	52.00	1087.00
22	SEG50	2537.20	2582.00	72	SEG0	52.00	972.00
23	SEG49	2537.20	2697.00	73	A0	52.00	857.00
24	SEG48	2537.20	2812.00	74	CS	52.00	742.00
25	SEG47	2537.20	2927.00	75	CL	52.00	627.00
26	SEG46	2537.20	3042.00	76	E(RD)	52.00	512.00
27	SEG45	2537.20	3157.00	77	R/W(WR)	52.00	397.00
28	SEG44	2537.20	3272.00	78	Vss	52.00	282.00
29	SEG43	2537.20	3387.00	79	DB0	52.00	167.00
30	SEG42	2537.20	3502.00	80	DB1	52.00	52.00
31	SEG41	2379.40	3512.10	81	DB2	198.40	52.00
32	SEG40	2264.40	3512.10	82	DB3	313.40	52.00
33	SEG39	2149.40	3512.10	83	DB4	428.40	52.00
34	SEG38	2032.20	3512.10	84	DB5	543.40	52.00
35	SEG37	1915.30	3512.10	85	DB6	658.40	52.00
36	SEG36	1800.30	3512.10	86	DB7	773.40	52.00
37	SEG35	1685.30	3512.10	87	Vdd	888.40	52.00
38	SEG34	1570.30	3512.10	88	RES	1003.40	52.00
39	SEG33	1455.30	3512.10	89	FR	1118.40	52.00
40	SEG32	1340.30	3512.10	90	V5	1233.40	52.00
41	SEG31	1225.30	3512.10	91	V3	1348.40	52.00
42	SEG30	1110.30	3512.10	92	V2	1463.40	52.00
43	SEG29	995.30	3512.10	93	M/S	1578.40	52.00
44	SEG28	880.30	3512.10	94	V4	1693.40	52.00
45	SEG27	760.40	3512.10	95	V1	1808.40	52.00
46	SEG26	629.60	3512.10	96	COM0	1923.40	52.00
47	SEG25	506.90	3512.10	97	COM1	2038.40	52.00
48	SEG24	387.50	3512.10	98	COM2	2153.40	52.00
49	SEG23	268.80	3512.10	99	COM3	2268.40	52.00
50	SEG22	150.80	3512.10	100	COM4	2383.40	52.00

6、PACKAGE INFORMATION

6. 1、QFP100-14×20-0.65





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D	22.00REF		
G1E	16.00REF		
L	0.60	0.80	1.00
L1	1.95REF		
θ	0°	2°	8°
θ 1	11°	13°	15°
θ 2	3°	5°	7°

7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

8、CONTACT：

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