AIP31086

80CH COMMON / SEGMENT DRIVER FOR DOT MATRIX LCD

1、GENERAL DESCRIPTION

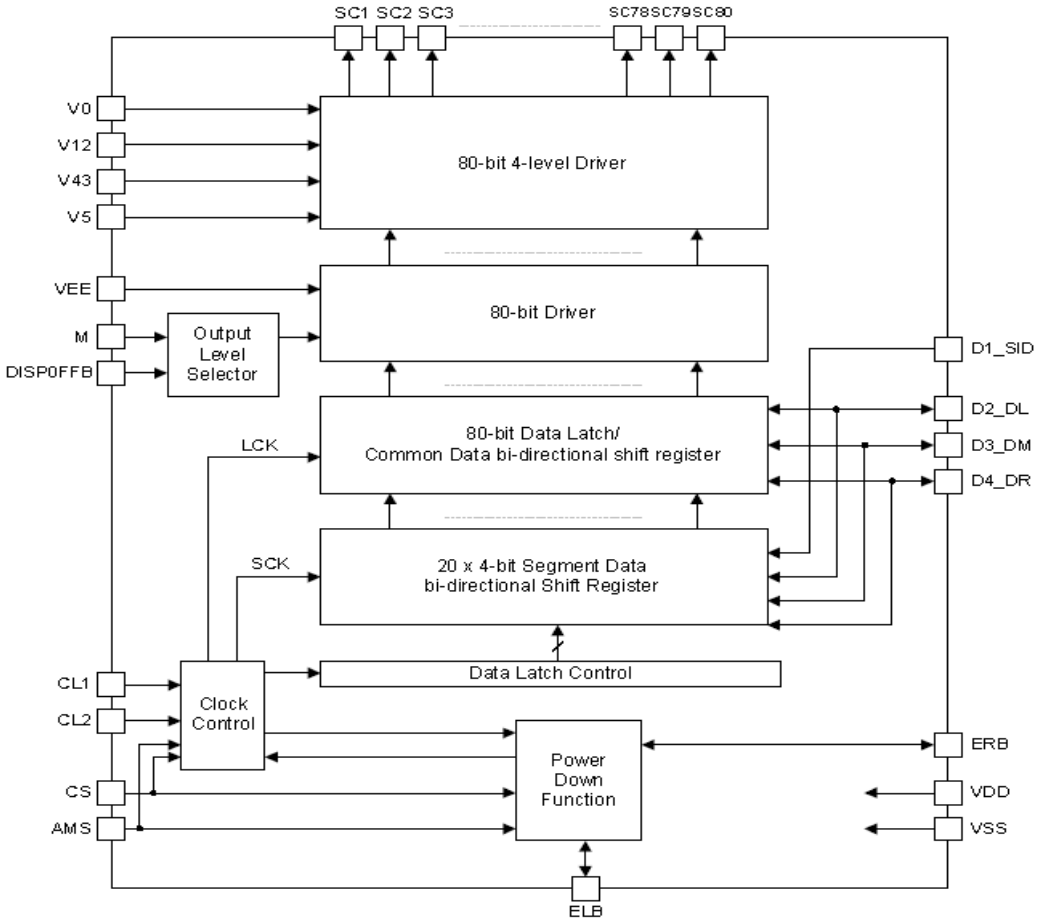
The AIP31086 is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

Features

- Power supply voltage: 3V ～ 5V
- Supply voltage for display: 6 to 23V (VDD-VEE)
- 4-bit parallel / 1-bit serial data processing (in segment mode)
- Single mode operation / dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty: 1/64 – 1/256
- High voltage CMOS process
- Chip size: 3920×3580 (μm×μm),
- The IC substrate should be connected to VDD or float in the PCB layout artwork.
- LQFP100 or bare chip available

2、BLOCK DIAGRAM AND BLOCK DESCRIPTION

2.1、BLOCK DIAGRAM

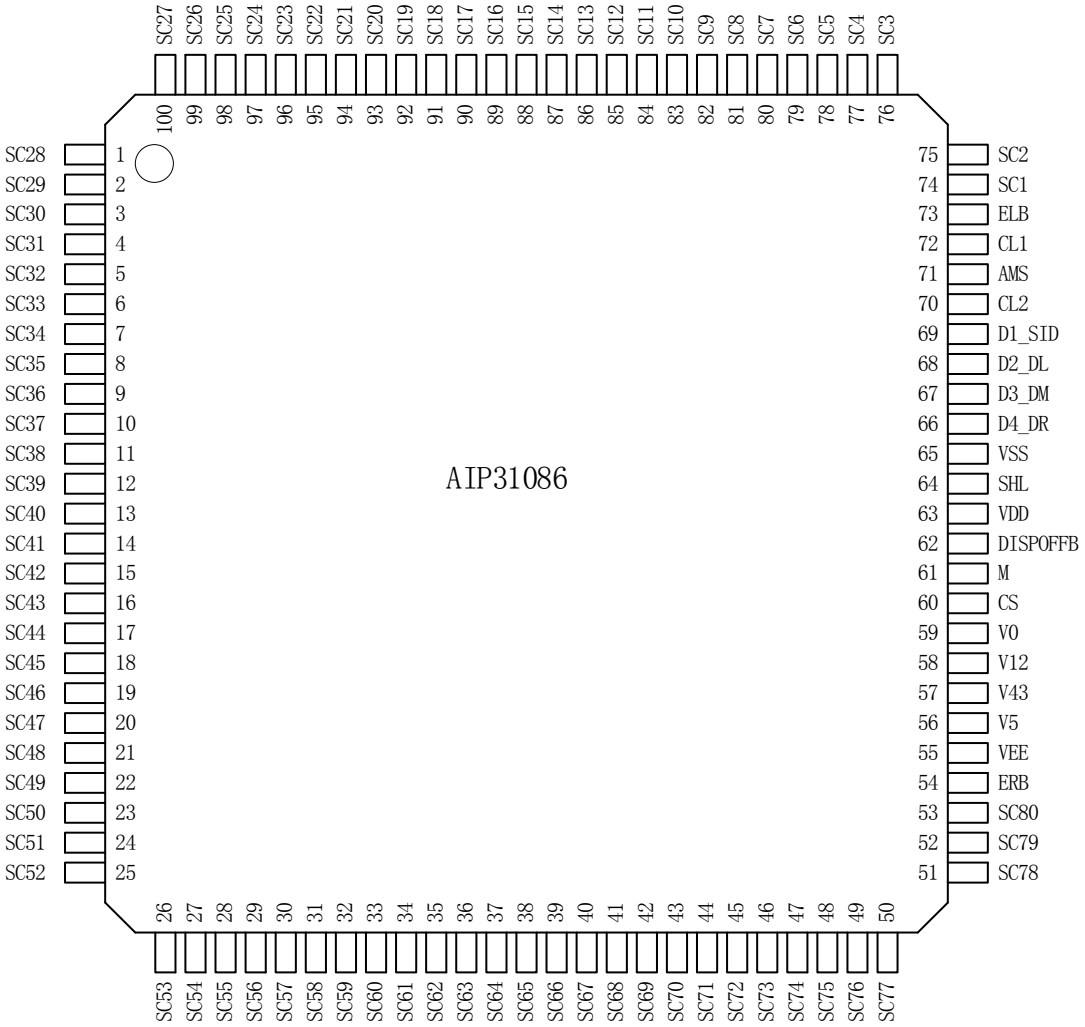


2.2、BLOCK DESCRIPTION

Name	Function	COM /SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM /SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is "Low", every clock of the current driver is enabled and the clock control block works. But if enable input is "High", current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB) (refer to PIN DESCRIPTION).	COM /SEG
20x4-bit segment data l-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch / common data l-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application,1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to NOTE 3).	COM /SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. and when in common driver application, this value becomes V1 or V4.	SEG

2.3 PIN CONFIGURATIONS

LQFP100



2.4、PIN DESCRIPTION

Pin No.	Pin Name		I / O	Description	Interface
63	VDD	Power supply		Logical "High" input port (+5V ±10%, +3V ±10%)	Power
65	VSS			0V (GND)	
55	VEE			Logical "Low" for high voltage part	
59 58 57 56	V0, V12, V43, V5	LCD driver output voltage level	I	Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to NOTE 2).	Power

<table>
<tr><td>1～53
74～
100</td><td>SC1 -
SC80</td><td>LCD
driver
output</td><td>O</td><td>Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>70</td><td>CL2</td><td>Data shift
clock</td><td>I</td><td>Clock pulse input for the bi-directional shift register. – In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid. – In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock. Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controll
er</td></tr>
<tr><td>61</td><td>M</td><td>AC signal
for LCD
driver
output</td><td>I</td><td>Alternate signal input pin for LCD driving. Normal frame inversion signal is input in to this pin.</td><td>Controll
er</td></tr>
<tr><td>72</td><td>CL1</td><td>Data latch
clock</td><td>I</td><td>– In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block. – In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controll
er</td></tr>
<tr><td>62</td><td>DISPOF
FB</td><td>Display
OFF
control</td><td>I</td><td>Control input pin to fix the driver output (SC1~SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controll
er</td></tr>
<tr><td>60</td><td>CS</td><td>COM /
SEG mode
control</td><td>I</td><td>When CS = "Low", AIP31086 is used as an 80-bit segment driver. When CS = "High", AIP31086 is set to an 80-bit common driver</td><td>VDD /
VSS</td></tr>
<tr><td>71</td><td>AMS</td><td>Applicatio
n
Mode
select</td><td>I</td><td>According to the input value of the AMS and the CS pin, application
mode of AIP31086 is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application Mode</th><th>COM/SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode</td><td rowspan="2"></td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode</td></tr>
<tr><td>1</td><td>0</td><td>Single type application mode</td><td>COM</td></tr>
</table></td><td>VDD /
VSS</td></tr>
</table>

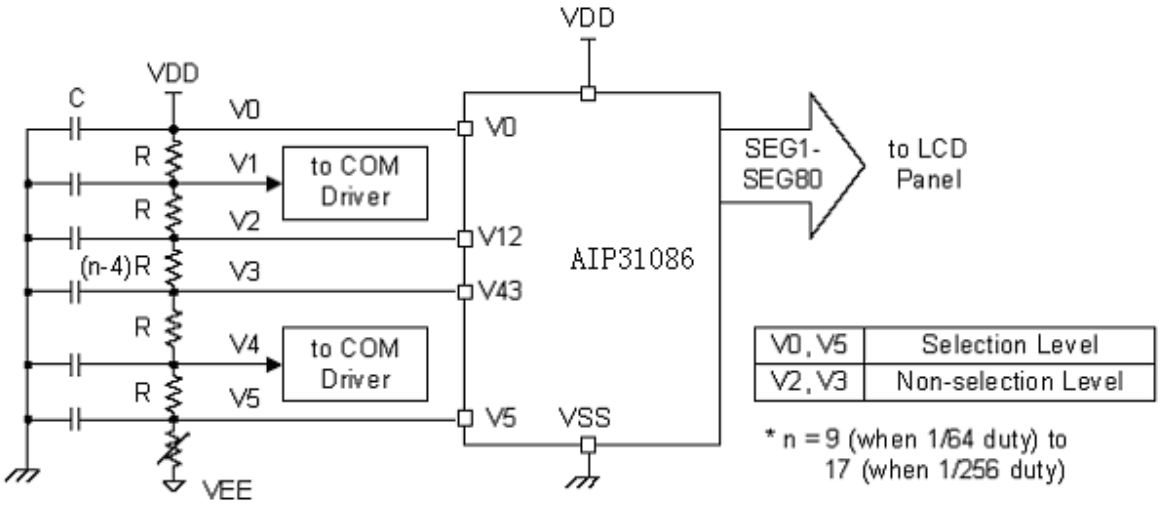
<table>
<tr><td></td><td></td><td></td><td></td><td><table><tr><td>1</td><td>1</td><td>Dual type application mode</td><td></td></tr></table></td><td></td></tr>
<tr><td>69
68
67
66</td><td>D1_SID,
D2_DL,
D3_DM,
D4_DR</td><td>Display data input / serial input data / left, right data input output</td><td>I / O</td><td>In segment driver application mode, these pins are
used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as
serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode : AMS = "High").
In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when in single type interface mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data
shift and the connection of data pins are determined
by SHL input (refer to NOTE 3, NOTE 4).</td><td>Controller</td></tr>
<tr><td>64</td><td>SHL</td><td>Shift direction control</td><td>I</td><td>When SHL = "Low", data is shifted from left to right. When SHL = "High", the direction is reversed. (refer to NOTE3)</td><td>VDD/VSS</td></tr>
<tr><td>73
54</td><td>ELB
ERB</td><td>Enable data Inpute/output</td><td>I/O</td><td>In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is “Low” (power down function). When several drivers are serially connected, the enable
state of each driver is shifted according to the SHL input. Connect these pins as below.<table><tr><td rowspan="2">SHL</td><td colspan="2">Segment Driver</td></tr><tr><td>ELB</td><td>ERB</td></tr><tr><td>L</td><td>Output(open)</td><td>Input(VSS)</td></tr><tr><td>H</td><td>Input(VSS)</td><td>Output(open)</td></tr></table>In common driver application mode, power down function is not used.
Open these pins.</td><td></td></tr>
</table>

NOTE 1. Output Level Control

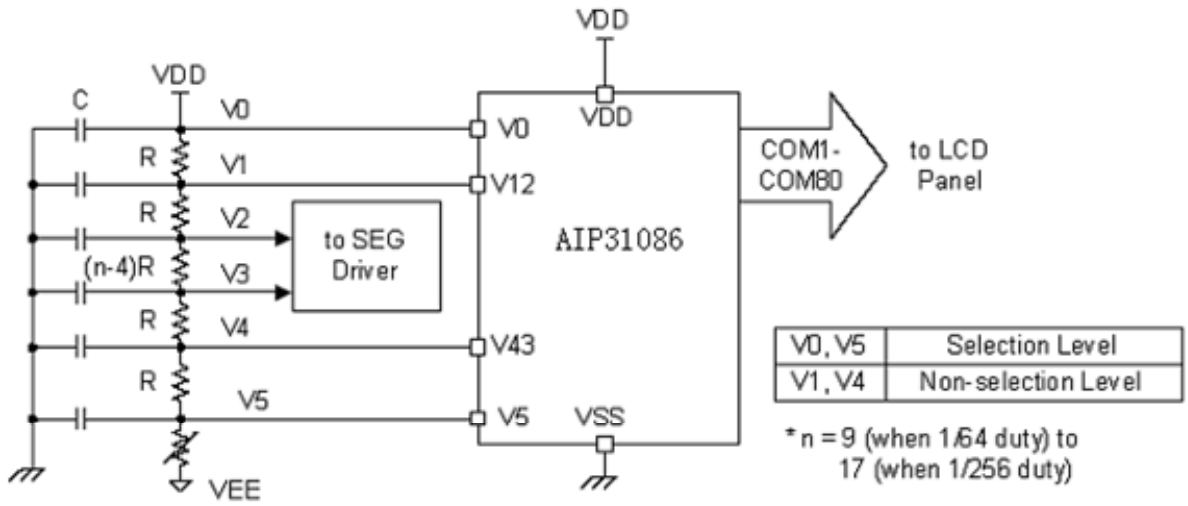
M	Latched data	DISPOFFB	Output level (SC1 –SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

NOTE 2. LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = "Low")

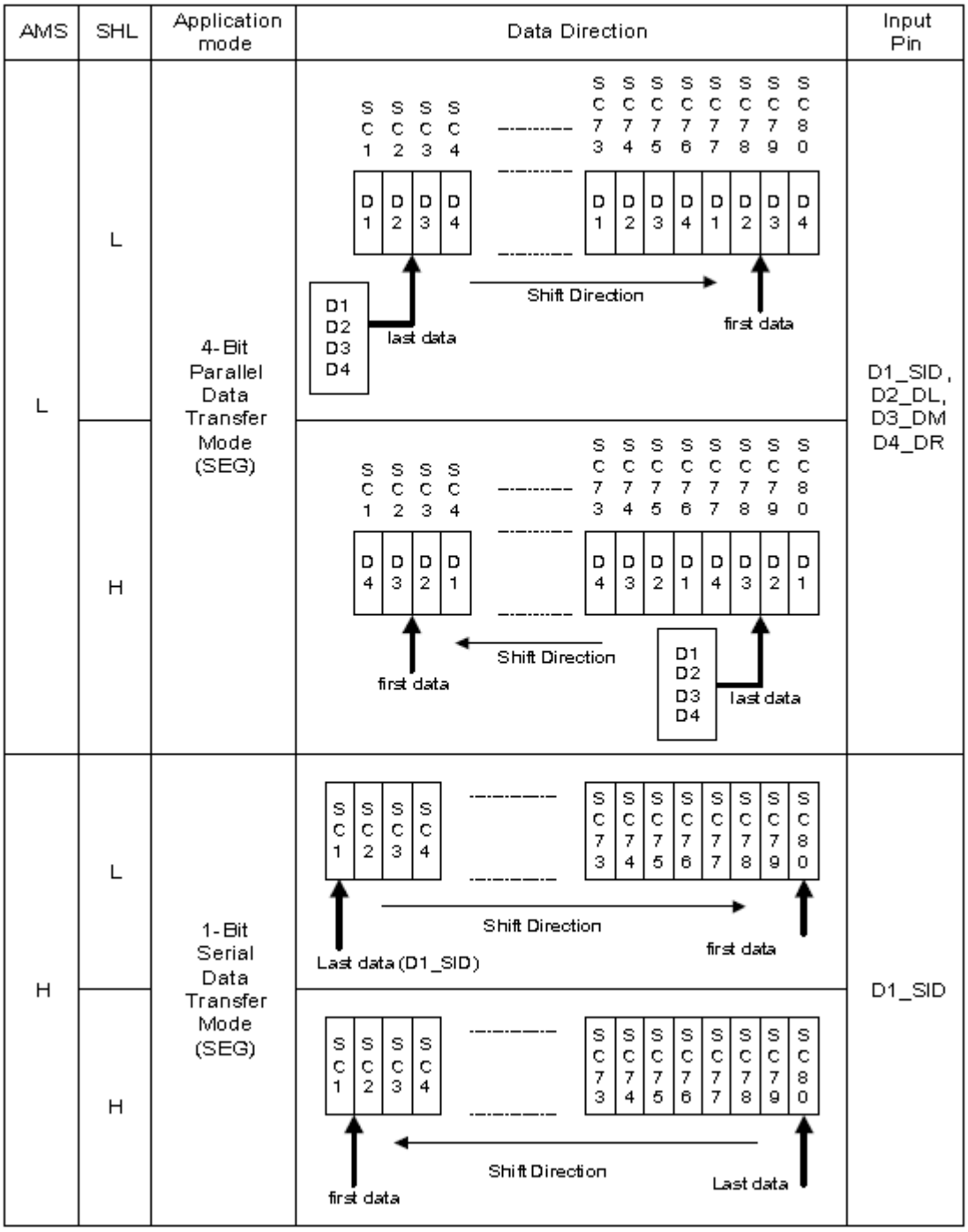


(2) Common driver application (CS = "High")

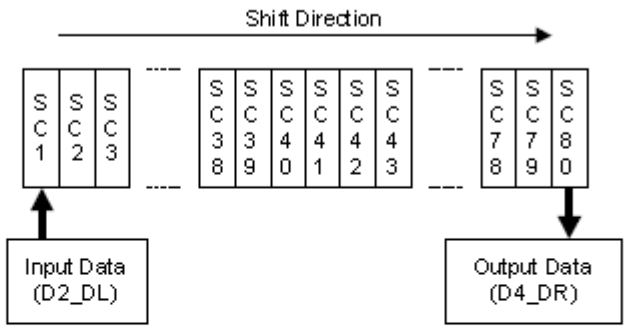
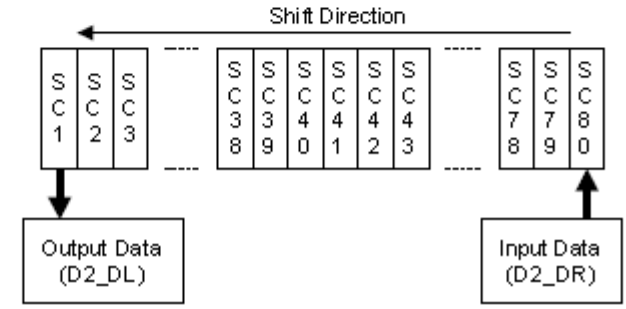
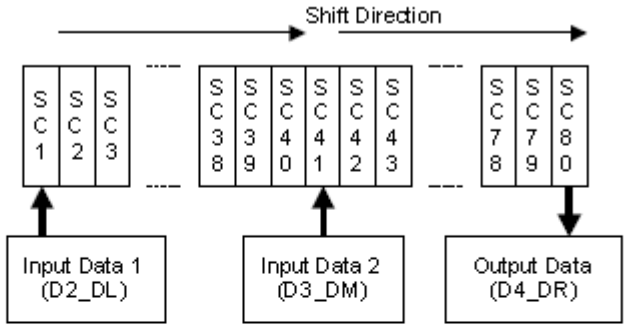
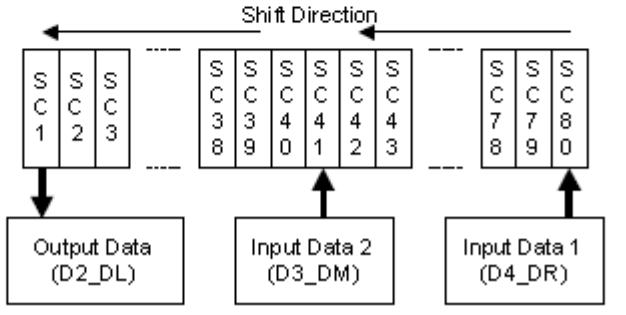


NOTE 3. Data Shift Direction according to Control Signals

(1) When CS = “Low” (segment driver application)



(2) When CS = “High” (common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

NOTE 4. Usage of Data Pins

COM / SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS ="Low")	4-bit parallel interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "High")	X	SID (input)	Connect to VDD		
COM (CS = "High")	single-type application mode (AMS = "Low")	L	open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS = "High")	L	open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}		-0.3 –+7.0	V
Driver supply voltage	V_{LCD}		0 –+25	V
Input voltage	V_{IN}		-0.3 –V_{DD}+ 0.3	V
Operating temperature	Topr		-30 –+85	℃
Storage temperature	Tstg		-55 –+150	℃
Soldering Temperature	T_L	10s	245	℃

* NOTE: Voltage greater than above may do damage to the circuit.

3.2、ELECTRICAL CHARACTERISTICS

3.2.1、DC CHARACTERISTICS

(1) Segment Driver Application (V_{SS} = 0V, Ta = - 30 – +85°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage1	V_{DD}	-	2.7	-	5.5	V
	V_{LCD}	V_{IN}= V_{DD}- V_{EE}	6	-	23	
Input voltage (1)	V_{IH}	-	0.8V_{DD}	-	V_{DD}	
	V_{IL}	-	0	-	0.2V_{DD}	
Output voltage (2)	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL}= 0.4mA	-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN}= $V_{DD}$to V_{SS}	-10	-	10	μA

Input leakage current 2 (3)	I_{IL2}	V_{IN}= $V_{DD}$to V_{EE}		-25	-	25	
On resistance (4)	R_{ON}	I_{ON}= 100μA		-	2	4	kΩ
Supply current (5)	I_{STBY}	f_{CL1}= 32kHz M = V_{SS}	V_{SS}pin	-	-	100	μA
	I_{DD}	f_{CL1}= 32kHz f_M= 80Hz	V_{DD} = 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} = 5V	-	-	500	μA

NOTES:

1. Applied to CL1, CL2, ELB, ERB, D1_SID - D4_DR, SHL, DISPOFFB, M, CS, AMS pin
2. ELB, ERB pin
3. V0, V12, V43, V5 pin
4. VLCD = VDD - VEE, V0 = VDD = 5V, V5= VEE = -23 V
   V12 = VDD-2/n(VLCD), V43 = VEE+2/n(VLCD), n = 17 (1/256 duty, 1/17 bias)
5. V0 = VDD, V12 = 1.71V(VDD = 5V) or -0.06V (VDD = 3V),
   V43 = -19.71 V(VDD = 5V) or -19.94V (VDD = 3V), V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias)
   4-bit parallel interface mode
   ISTBY : VDD = 5V, fCL2 = 5.12MHz, SHL = VSS, DISPOFFB = VDD,
   M = VSS, display data pattern = 0000
   IDD : VDD = 3V, fCL2 = 4MHz, display data pattern = 0101
   VDD = 5 V, fCL2 = 5.12MHz, display data pattern = 0101
   IEE : VDD = 5V, fCL2 = 5.12MHz, display data pattern = 0101, VEE pin

(2) Common Driver Applicatio (V_{SS} = 0V, Ta = - 30 – +85°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.7	-	5.5	V
	V_{LCD}	V_{IN}= V_{DD}- V_{EE}	6	-	23	
Input voltage (1)	V_{IH}	-	0.8V_{DD}	-	V_{DD}	
	V_{IL}	-	0	-	0.2V_{DD}	
Output voltage (3)	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL}= 0.4mA	-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN}= $V_{DD}$to V_{SS}	-10	-	10	μA
Input leakage current 2 (2)	I_{IL2}	V_{IN}= 0V, V_{DD}= 5V (PULL UP)	-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN}= $V_{DD}$to V_{EE}	-25	-	25	
On	R_{ON}	I_{ON}= 100μA	-	2	4	kΩ

resistance(5)							
Supply current (6)	I_{STBY}	f_{CL1}= 32kHz	Vsspin	-	-	100	μA
	I_{DD}	f_{CL1}= 32kHz f_M= 80Hz	V_{DD} = 5V	-	-	200	
			V_{DD} = 3V	-	-	120	
	I_{EE}		V_{DD} = 5V	-	-	150	

NOTES:

1. Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
2. Pull-up input pins : CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
3. D2_DL (SHL = HIGH) , D4_DR (SHL = LOW) pin
4. V0, V12, V43, V5 pin
5. VLCD = VDD-VEE, V0 = VDD = 5V, V5 = VEE = -23V
   V12 = VDD-1/n(VLCD), V43 = VEE+1/n(VLCD), n = 17(1/256 duty, 1/17 bias)
6. V0 = VDD, V12 = 3.35V (VDD = 5V) or 1.47V (VDD = 3V),
   V43 = -21.35V (VDD = 5 V) or -21.47V (VDD = 3 V), V5 = VEE = -23 V, no-load condition (1/256 duty, 1/17 bias)
   single-type mode operation : AMS = VSS, SHL = VSS, DISPOFFB = VDD
   D1_SID = D3_DM = VDD, D4_DR = OPEN, ELB = ERB = OPEN,
   ISTBY : VDD = 5V, M = VSS, D2_DL = VSS
   IDD : fM = 80Hz, D2_DL = VDD
   VDD = 3 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   VDD = 5 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   IEE : fM = 80Hz, D2_DL = VDD
   VDD = 5V, current through VEE Pin,
   display data pattern = 10000000..., 01000000...,00100000..., 00010000...

3.2.2、AC CHARACTERISTICS

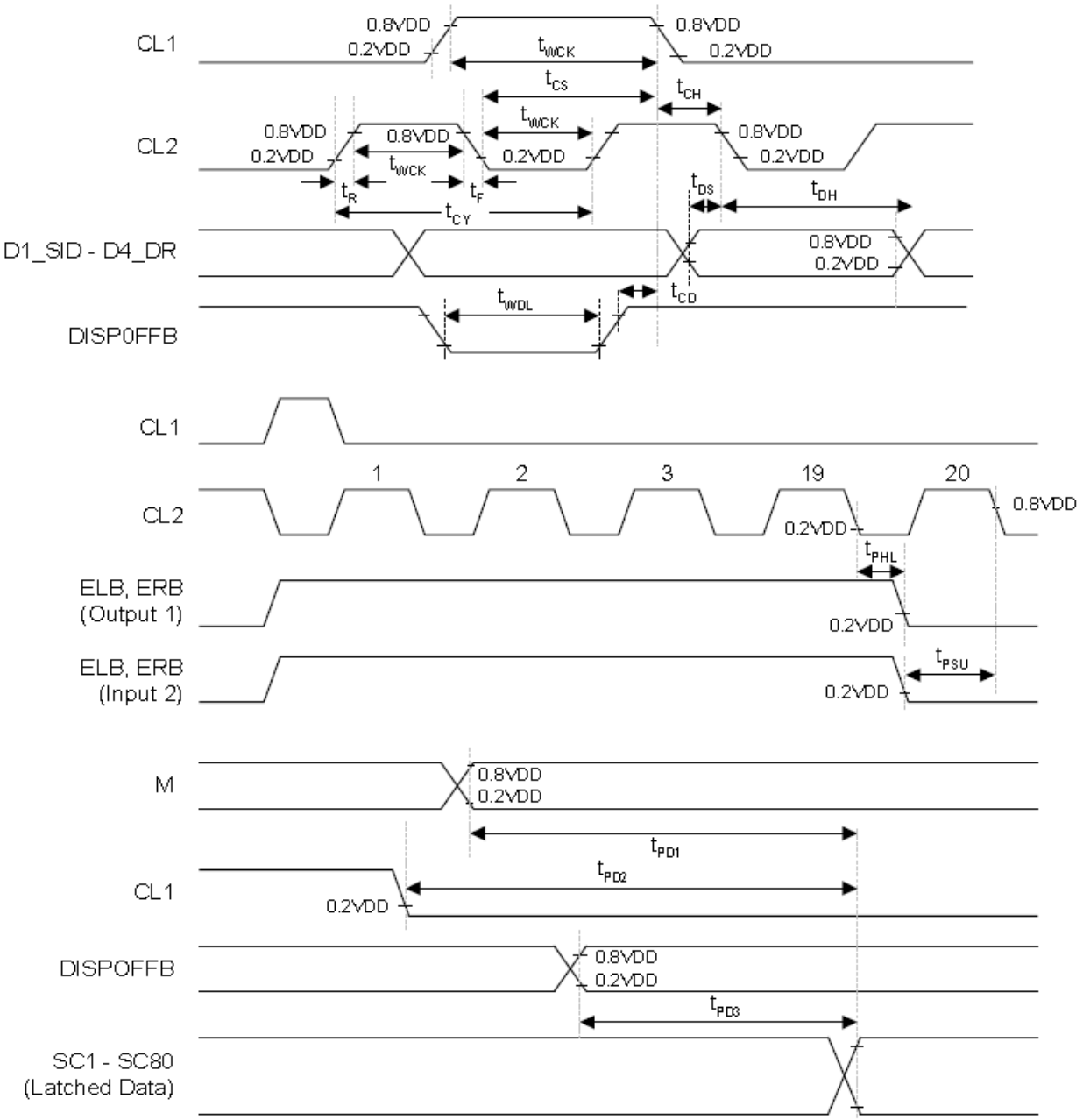
(1) Segment Driver Application (VSS = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Conditio	(1) V_{DD} = 5V 10%			(2) V_{DD} = 3V 10%			Unit
			Min.	Typ.	Ma.	Min.	Typ	Max.	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	tR/tF	-	-	-	-	-	-	30	
Data set-up time	tDS	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	tCS	-	80	-	-	120	-	-	
Clock hold time	tCH	-	80	-	-	120	-	-	
Propagation delay time	tPHL	ELB Output	-	-	60	-	-	125	
		ERB Output	-	-	60	-	-	125	
ELB,ERB set-up time	tPSU	ELB Input	30	-	-	65	-	-	
		ERB Input	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	s
DISPOFFB clear time	tCD	-	100	-	-	100	-	-	ns
M - OUT propagation delay time	tPD1	CL = 15pF	-	-	1.0	-	-	1.2	μs
CL1 - OUT propagation delay time	tPD2		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	tPD3		-	-	1.0	-	-	1.2	

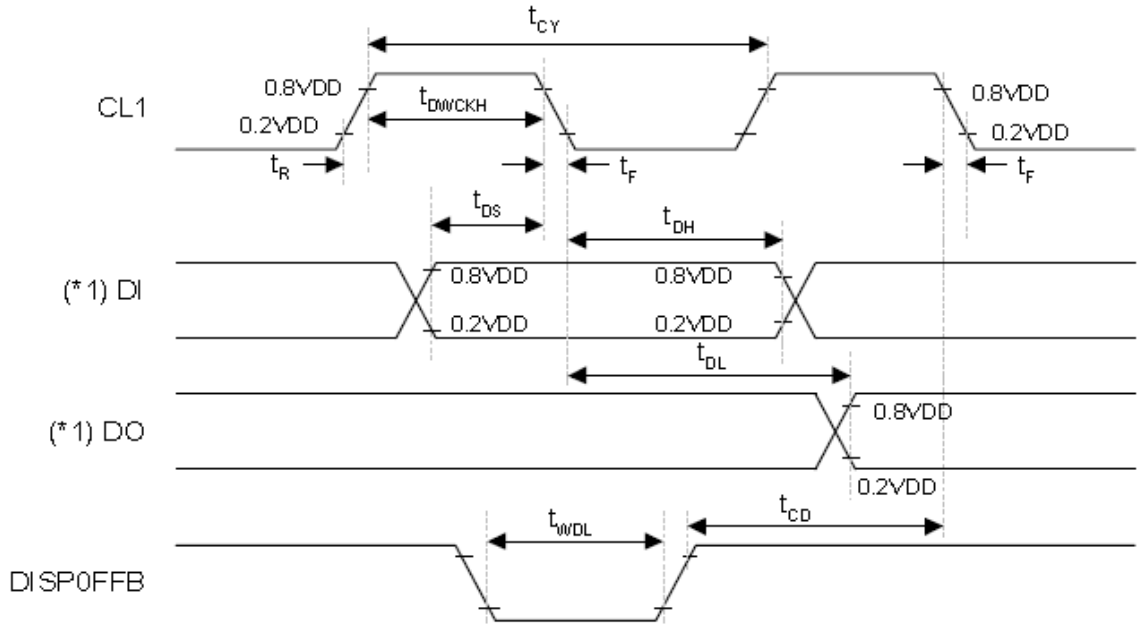
(2) Common Driver Application (VSS = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Conditio	(1) V_{DD} = 5V 10%			(2) V_{DD} = 3V 10%			Unit
			Min.	Typ.	Max	Min.	Typ	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	tR/tF	-	-	-	50	-	-	50	
Data set-up time	tDS	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	tCD	-	100	-	-	100	-	-	ns
Output delay time	tDL	CL = 15pF	-	-	200	-	-	250	ns
M - OUT propagation delay time	tPD1		-	-	1.0	-	-	1.2	μs
CL1 - OUT propagation delay time	tPD2		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	tPD3		-	-	1.0	-	-	1.2	

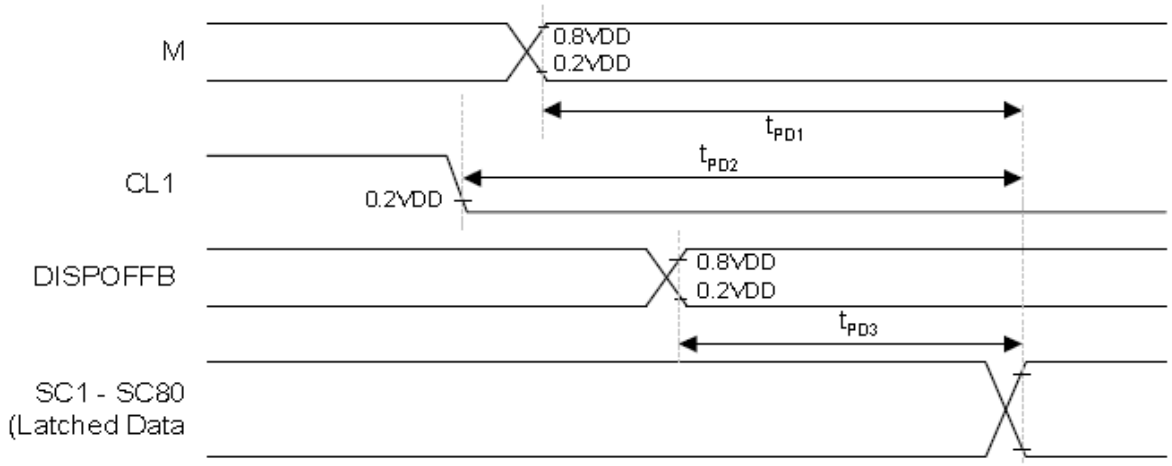
(3) Segment Driver Application Timing



(4) Common Driver Application Timing

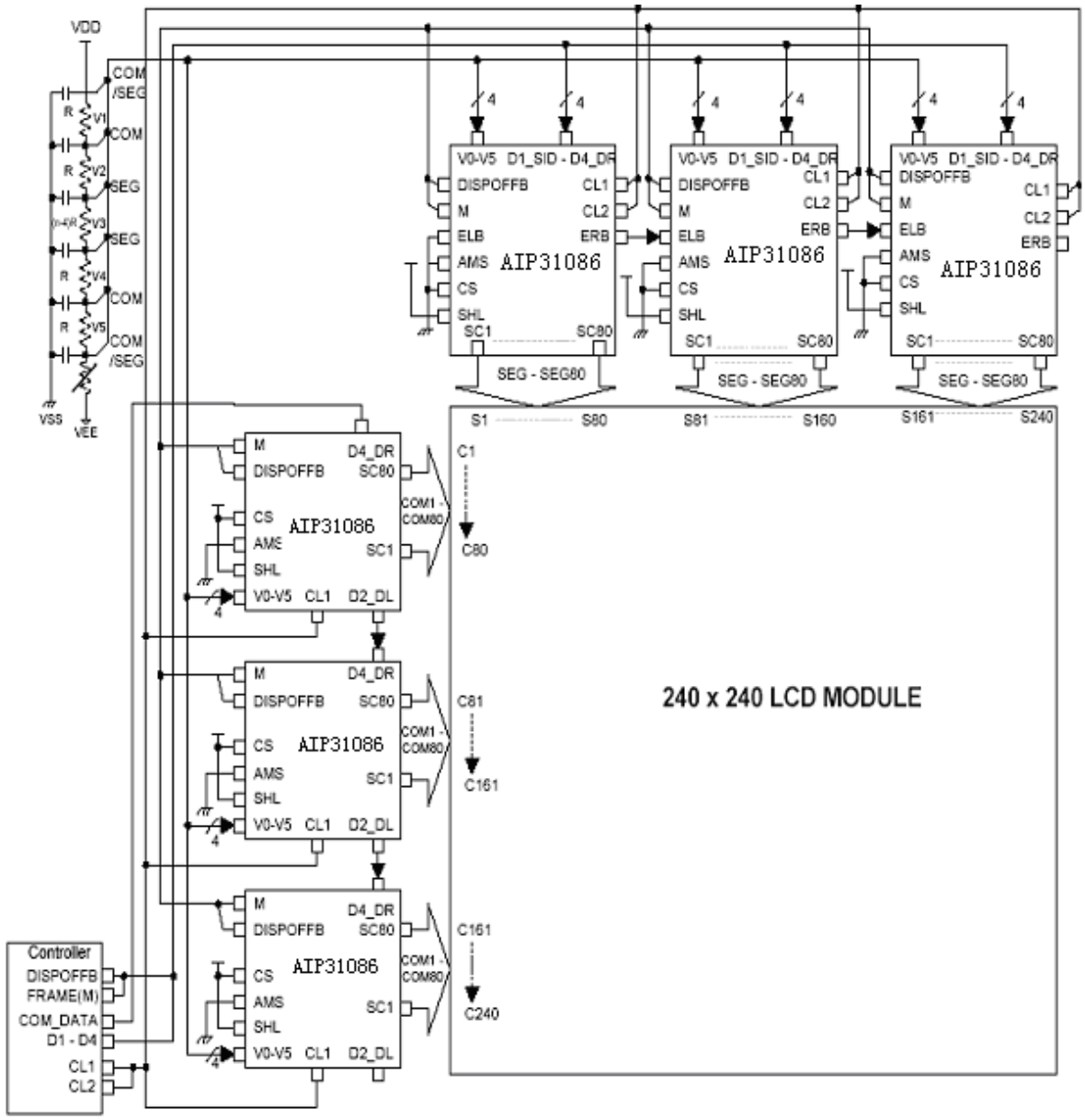


(*1) When in single-type interface mode
DI => D2_DL (SHL = L), D4_DR (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)
When in dual-type interface mode
DI => D2_DL and D3_DM (SHL = L), D4_DR and D3_DM (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)



4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT



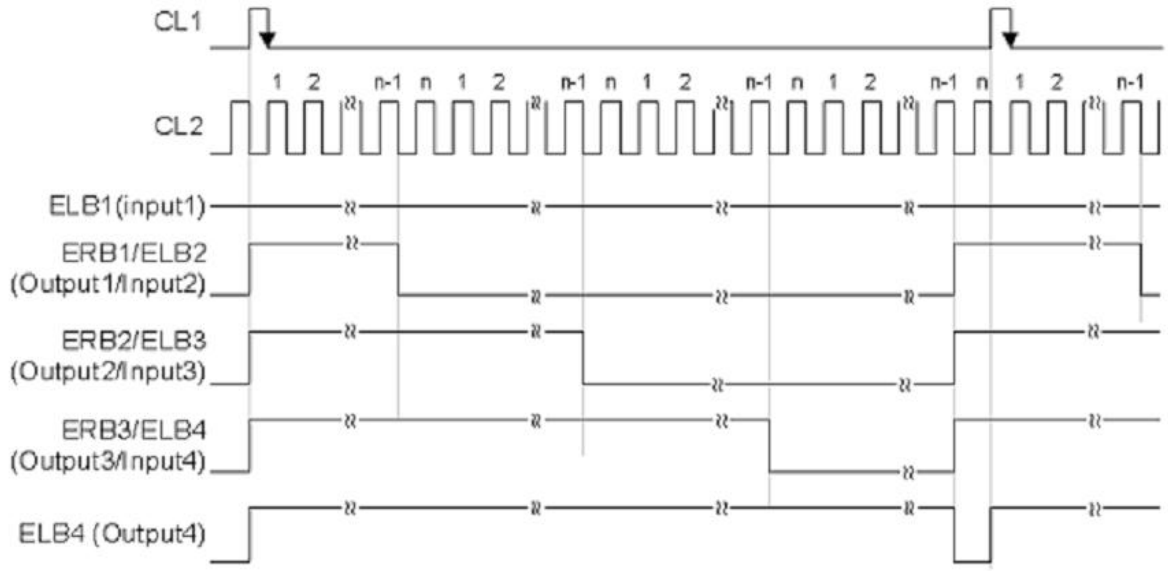
4. 2、APPLICATION NOTE

POWER DOWN FUNCTION

In the case of cascade connection of segment mode drivers, AIP31086 has a "power down function" In order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB ="Low", current driver is enabled.	Disabled
H	ELB	ERB	While ELB ="Low", current driver is enabled.	Disabled

* In the case of common driver application, power down function does not work.



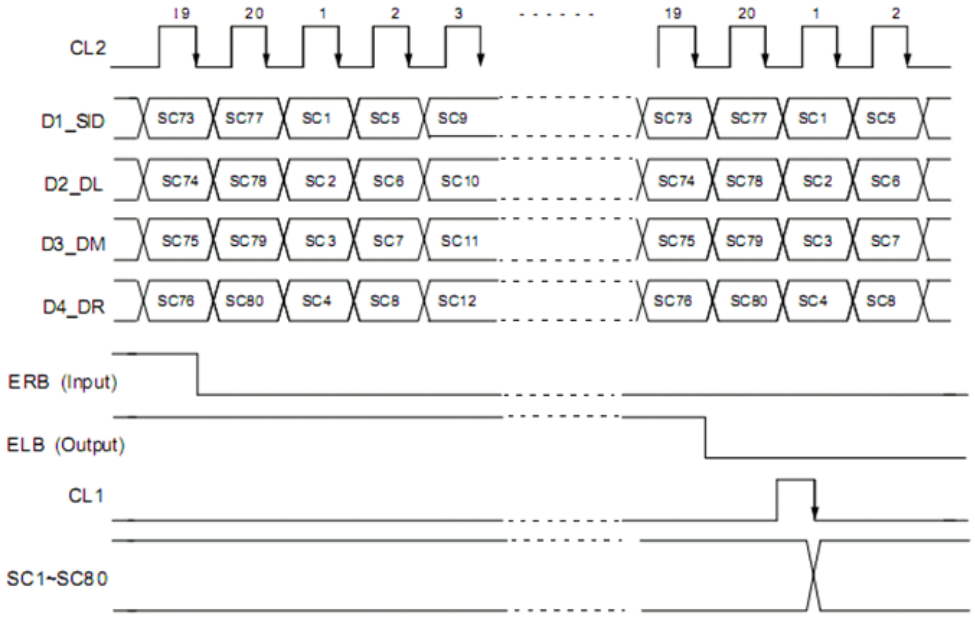
Notes:

1. SHL=High (EBL=Input, ERB=Output)
   Current AIP31086'S ERB must be connected to the next AIP31086'S ELB.
2. When in 4-bit parallel interface mode: n=20
   When in 1-bit serial interface mode: n=80

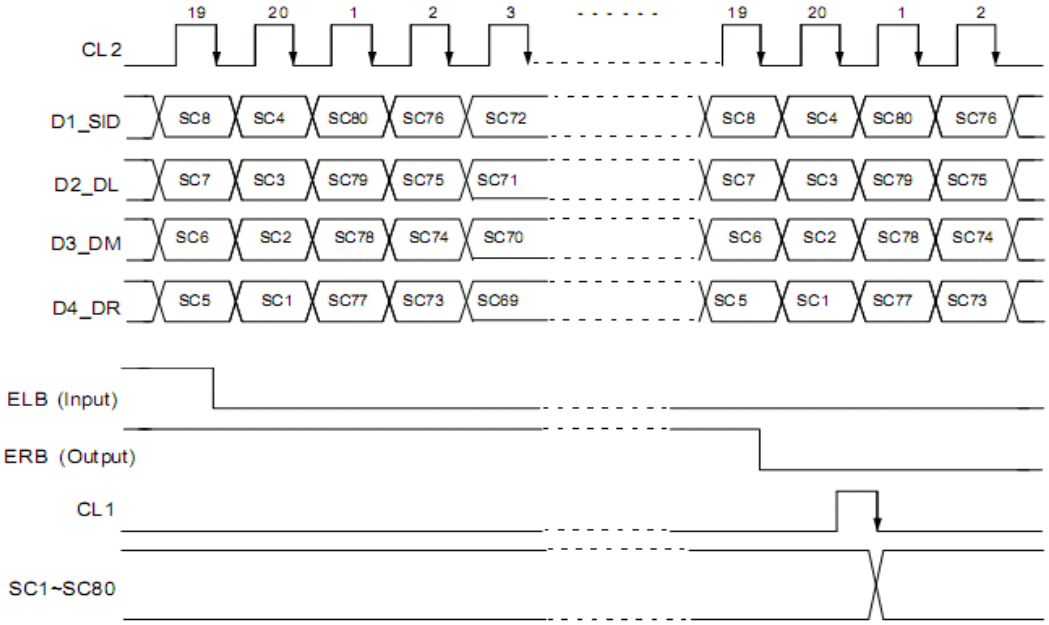
OPERATION TIMING DIAGRAM

(1) 4-bit Parallel Mode Interface Segment Driver

- When SHL = "Low"

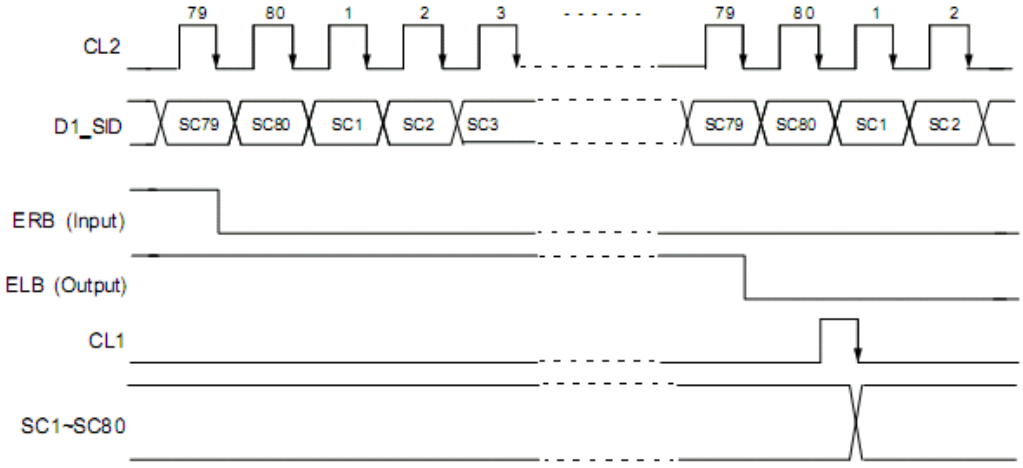


- When SHL = "High"

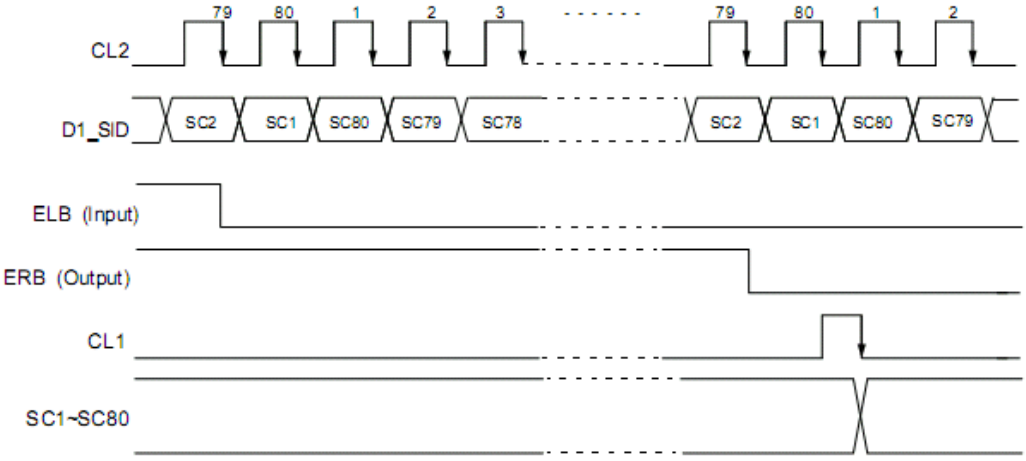


(2) 1-bit Serial Mode Interface Segment Driver

- When SHL = “Low”

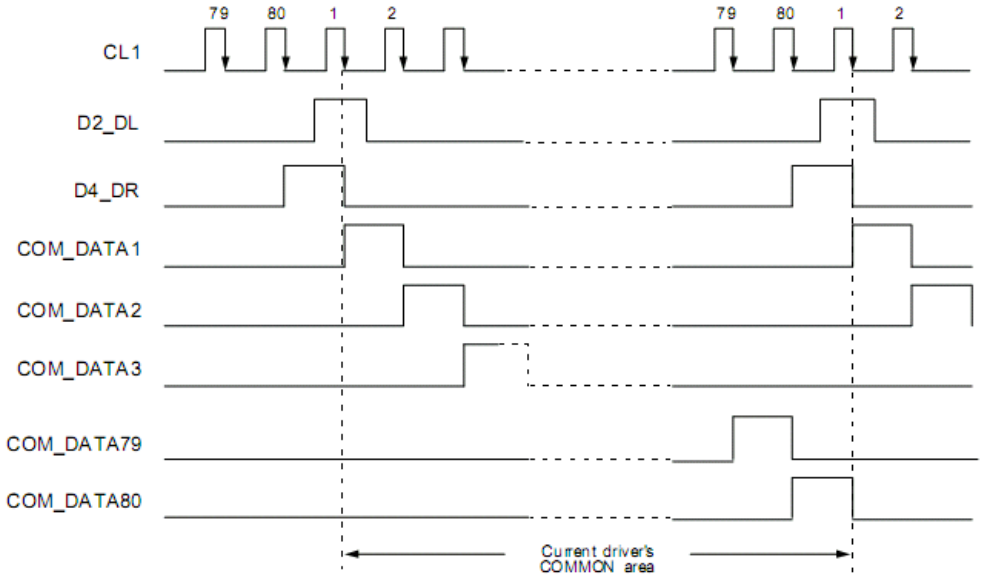


- When SHL = “High”

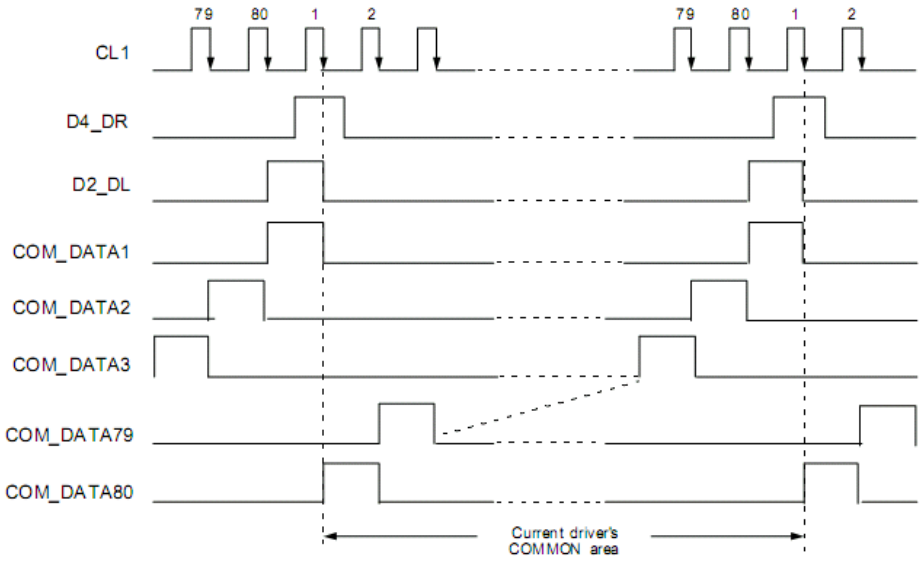


(3) Single-type Interface Mode Common Driver

- When SHL = “Low”

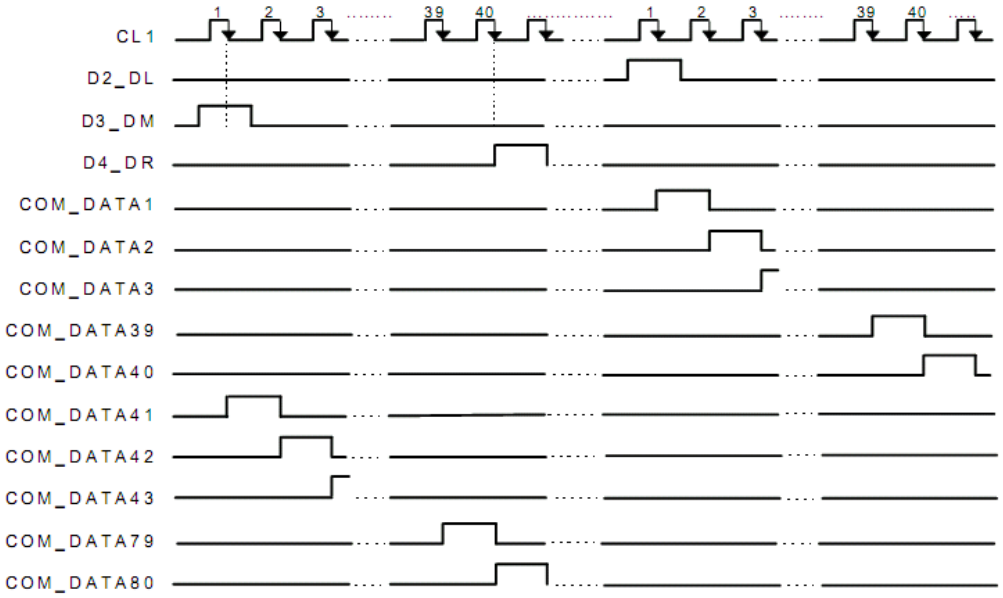


- When SHL = “High”

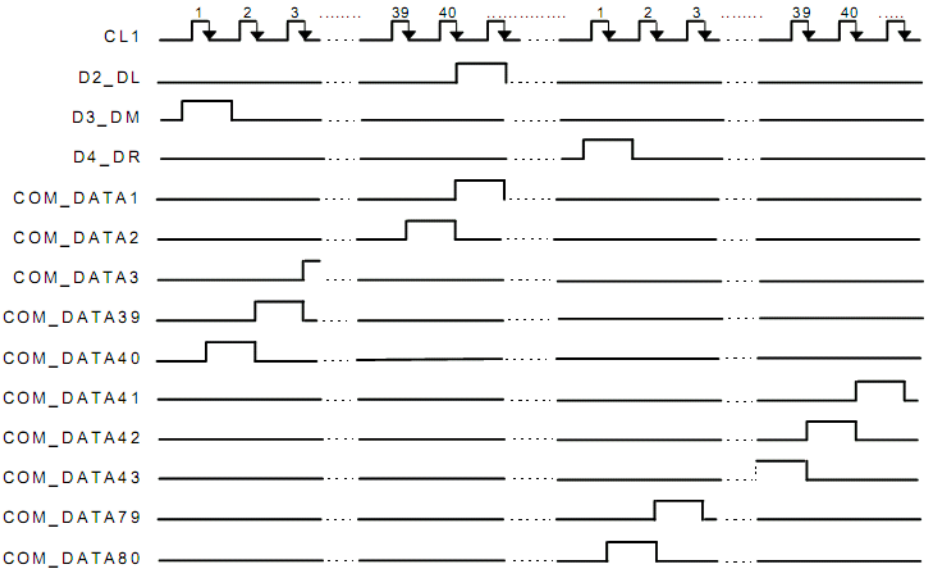


(4) DUAL-type Interface Mode Common Driver

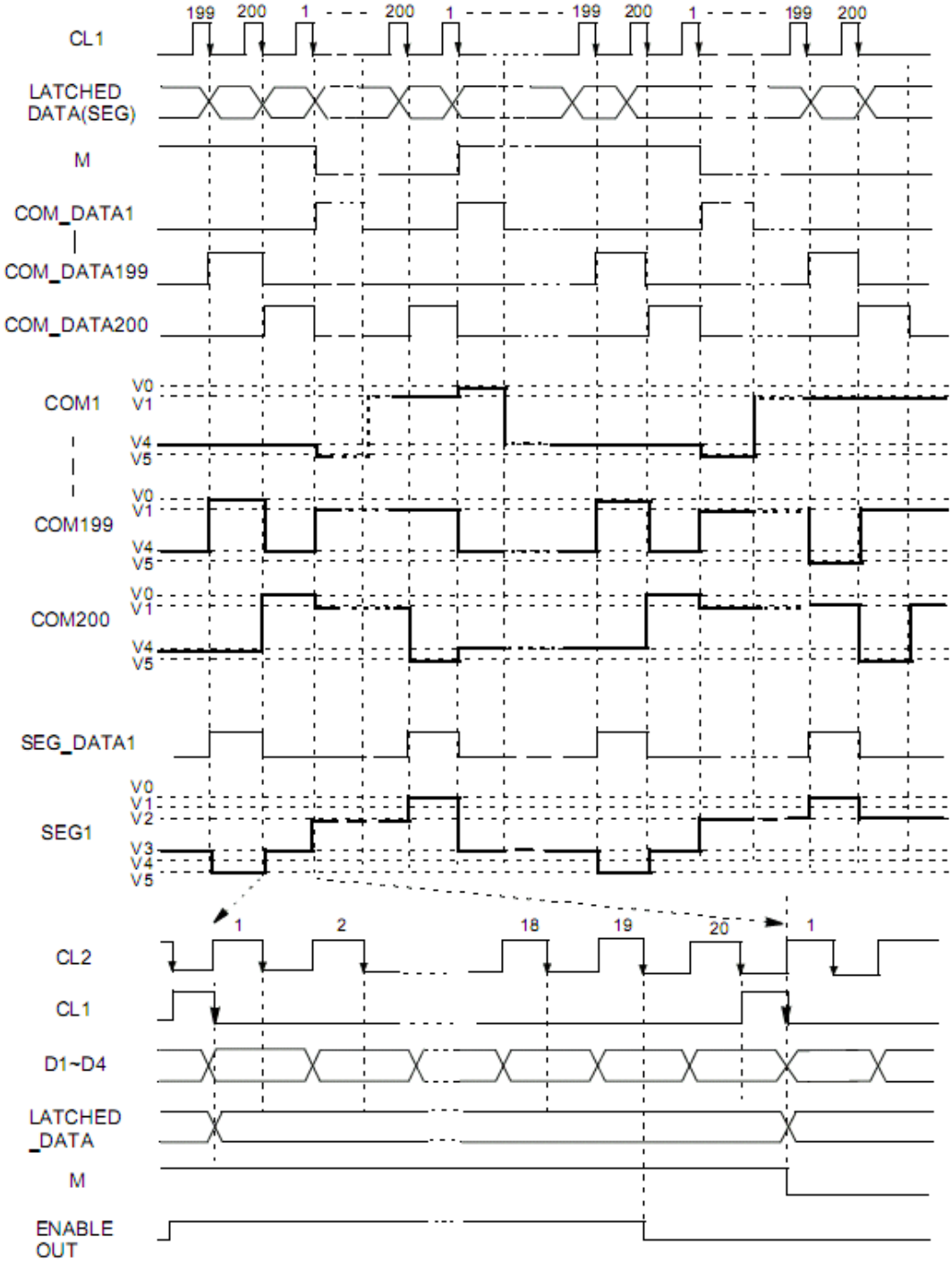
- When SHL = “Low”



- When SHL = “High”

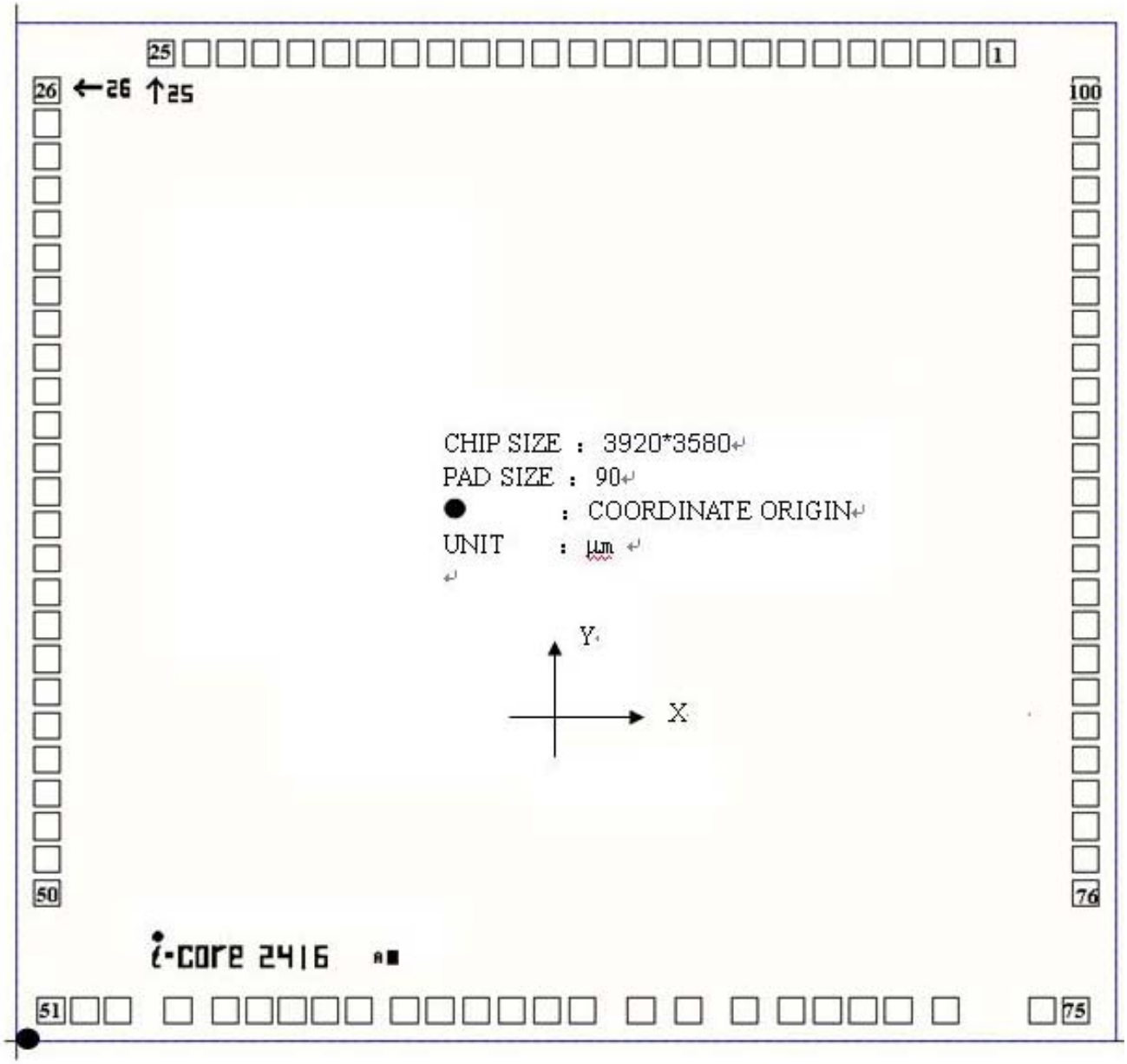


(5) Common / Segment Driver Timing (1/200 DUTY)



5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM



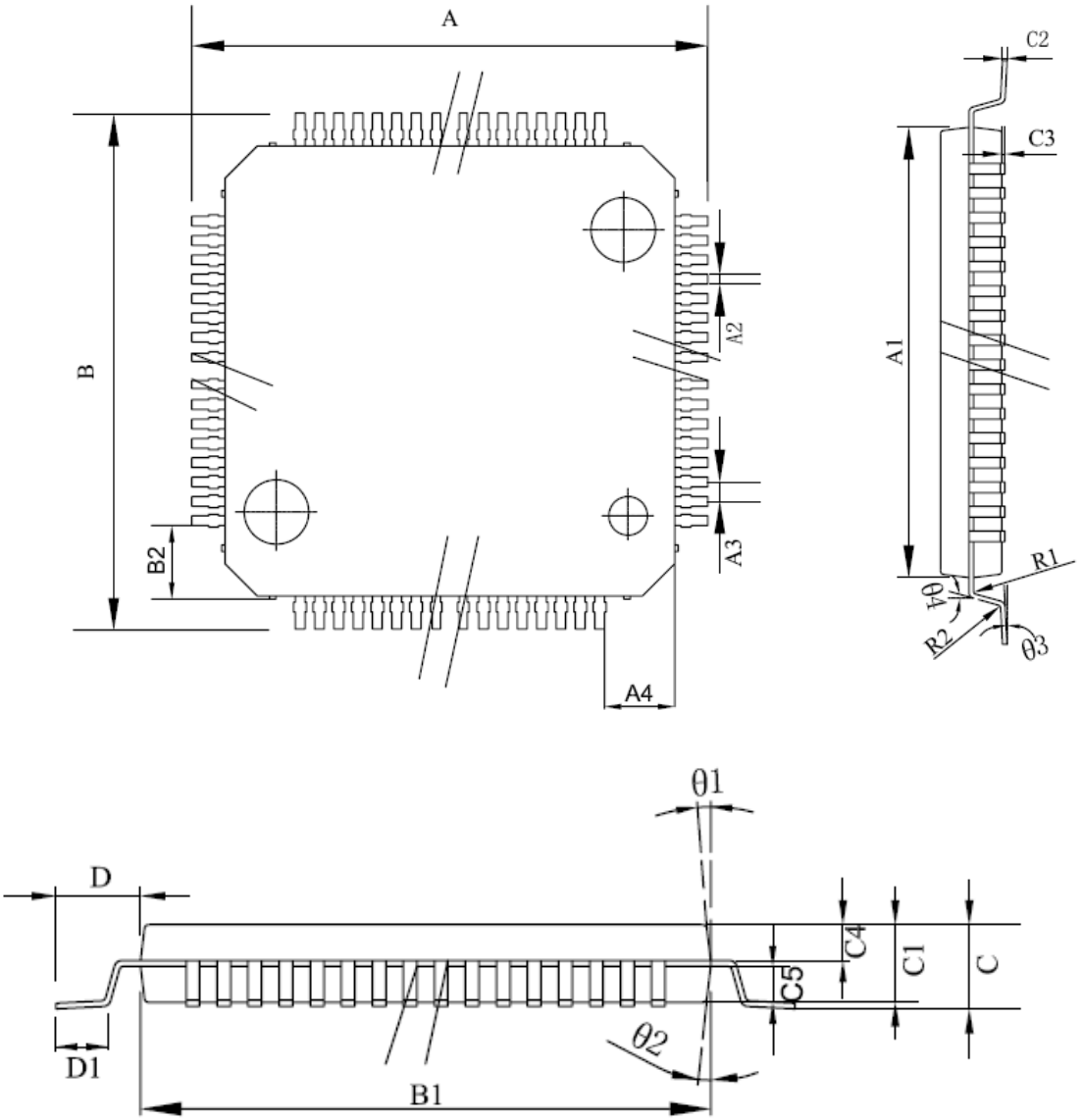
5.2、PAD Location （UNIT:μm）

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	SC28	3385.00	3392.55	51	SC78	119.15	104.00
2	SC29	3265.00	3392.55	52	SC79	234.15	104.00
3	SC30	3145.00	3392.55	53	SC80	349.15	104.00
4	SC31	3025.00	3392.55	54	ERB	556.15	104.00
5	SC32	2905.00	3392.55	55	VEE	717.55	104.00
6	SC33	2785.00	3392.55	56	V5	832.55	104.00
7	SC34	2665.00	3392.55	57	V43	947.55	104.00
8	SC35	2545.00	3392.55	58	V12	1062.55	104.00
9	SC36	2425.00	3392.55	59	V0	1177.55	104.00
10	SC37	2305.00	3392.55	60	CS	1334.55	104.00
11	SC38	2185.00	3392.55	61	M	1456.55	104.00
12	SC39	2065.00	3392.55	62	DISPOFFB	1578.55	104.00
13	SC40	1945.00	3392.55	63	VDD	1700.55	104.00
14	SC41	1818.00	3392.55	64	SHL	1822.55	104.00
15	SC42	1698.00	3392.55	65	GND	1944.55	104.00
16	SC43	1578.00	3392.55	66	D4	2146.55	104.00
17	SC44	1458.00	3392.55	67	D3	2309.95	104.00
18	SC45	1338.00	3392.55	68	D2	2501.95	104.00
19	SC46	1218.00	3392.55	69	D1	2665.35	104.00
20	SC47	1098.00	3392.55	70	CL2	2787.35	104.00
21	SC48	978.00	3392.55	71	AMS	2909.35	104.00
22	SC49	858.00	3392.55	72	CL1	3031.35	104.00
23	SC50	738.00	3392.55	73	ELB	3192.75	104.00
24	SC51	618.00	3392.55	74	SC1	3525.15	104.00
25	SC52	498.00	3392.55	75	SC2	3640.15	104.00
26	SC53	103.20	3267.05	76	SC3	3676.80	507.05
27	SC54	103.20	3152.05	77	SC4	3676.80	622.05
28	SC55	103.20	3037.05	78	SC5	3676.80	737.05
29	SC56	103.20	2922.05	79	SC6	3676.80	852.05
30	SC57	103.20	2807.05	80	SC7	3676.80	967.05
31	SC58	103.20	2692.05	81	SC8	3676.80	1082.05
32	SC59	103.20	2577.05	82	SC9	3676.80	1197.05
33	SC60	103.20	2462.05	83	SC10	3676.80	1312.05
34	SC61	103.20	2347.05	84	SC11	3676.80	1427.05
35	SC62	103.20	2232.05	85	SC12	3676.80	1542.05
36	SC63	103.20	2117.05	86	SC13	3676.80	1657.05
37	SC64	103.20	2002.05	87	SC14	3676.80	1772.05
38	SC65	103.20	1887.05	88	SC15	3676.80	1887.05
39	SC66	103.20	1772.05	89	SC16	3676.80	2002.05

40	SC67	103.20	1657.05	90	SC17	3676.80	2117.05
41	SC68	103.20	1542.05	91	SC18	3676.80	2232.05
42	SC69	103.20	1427.05	92	SC19	3676.80	2347.05
43	SC70	103.20	1312.05	93	SC20	3676.80	2462.05
44	SC71	103.20	1197.05	94	SC21	3676.80	2577.05
45	SC72	103.20	1082.05	95	SC22	3676.80	2692.05
46	SC73	103.20	967.05	96	SC23	3676.80	2807.05
47	SC74	103.20	852.05	97	SC24	3676.80	2922.05
48	SC75	103.20	737.05	98	SC25	3676.80	3037.05
49	SC76	103.20	622.05	99	SC26	3676.80	3152.05
50	SC77	103.20	507.05	100	SC27	3676.80	3267.05

6、PACKAGE INFORMATION

6. 1、 LQFP100



尺寸 / 标注	最小（mm）	最大（mm）	尺寸 / 标注	最小（mm）	最大（mm）
A	15.80	16.20	C3	0.05	0.15
A1	13.90	14.10	C4	0.6365TYP	
A2	0.17	0.27	C5	0.6365TYP	
A3	0.5TYP		D	0.90	1.10
A4	0.9TYP		D1	0.45	0.70
B	15.80	16.20	R1	0.15TYP	
B1	13.90	14.10	R2	0.15TYP	
B2	0.9TYP		θ1	12° TYP	
C	1.40	1.60	θ2	12° TYP	
C1	1.35	1.45	θ3	4° TYP	
C2	0.09	0.18	θ4	4° TYP	

7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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