AIP31066

16COM / 40SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

1、GENERAL DESCRIPTION

AIP31066 is a dot matrix LCD driver & controller LSI whichis fabricated by low power CMOS technology.

It can display 1or 2 lines with the 5×8 dots format or 1 line with the 5×11 dots format.

Features

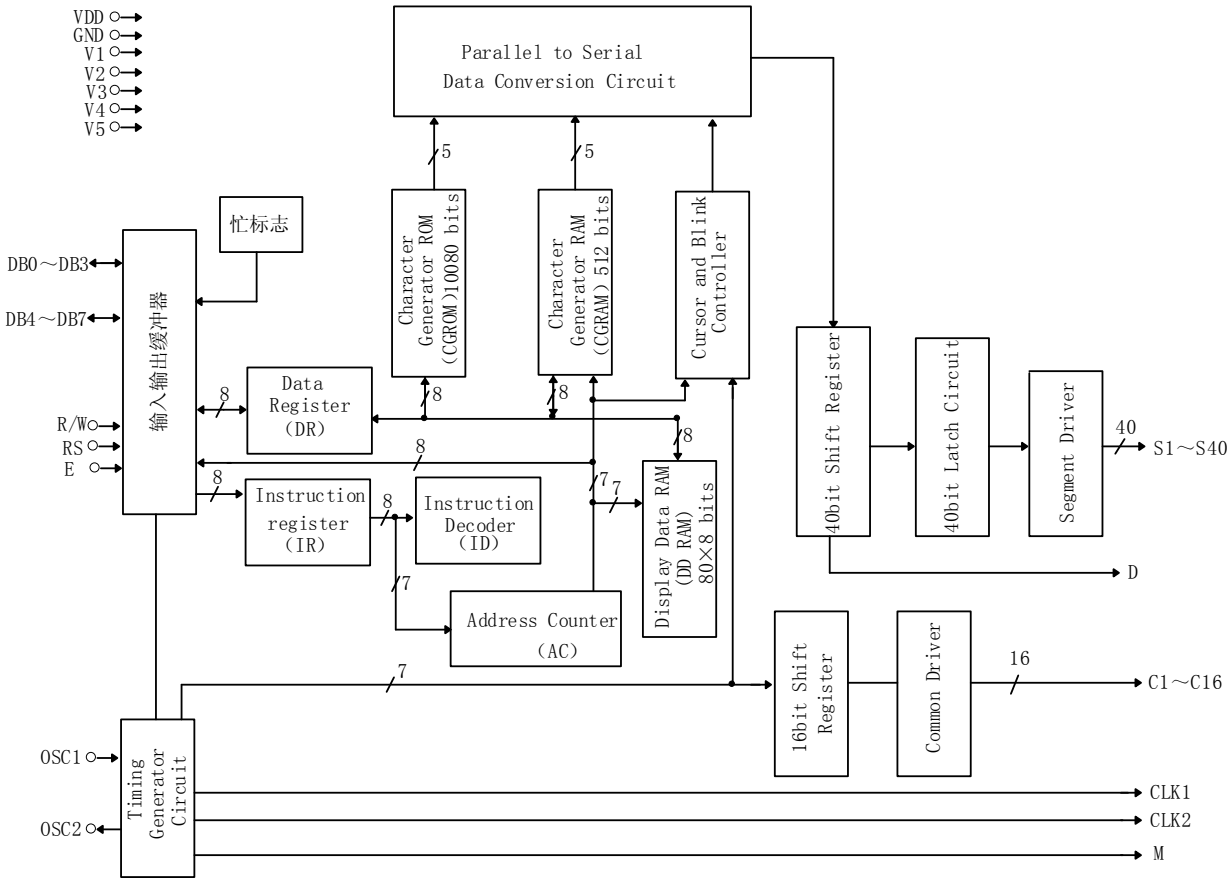
• Character type dot matrix LCD driver & controller.
• Internal driver: 16 common and 40 segment signal output.
• Easy interface with 4-bit or 8-bit MPU.
• Display character pattern: 5×8 dots format (208 kinds) & 5×11 dots format (32 kinds).
• The Special character pattern is directly programmable by the Character Generator RAM.
• A customer character pattern is programmable by mask option.
• Programmable Driving Method by the same character font mask option: Display Waveform A-type
• It can drive a maximum at 80 characters by using the AIP31065 or AIP31063 externally.
• Various instruction functions.
• Built-in automatic power on reset.
•Internal Memory
- Character Generator ROM (CGROM): 10,080 bits (204 characters×5×8 dots) & (32 characters×5×11 dots)
- Character Generator RAM (CGRAM): 64×8 bits (8 characters×5×8 dots)
- Display Data RAM (DDRAM): 80×8 bits (80 characters max.)
• Low power operation
- Power supply voltage range (VDD): 2.7 to 5.5 V
- LCD Drive voltage range (VDD-V5): 3.0 to 13.0 V
• CMOS process
• Programmable duty cycle: 1/8, 1/11, 1/16
• Internal oscillator with external resistor
• Low power consumption
• Chip size: 3240×3020 (um×um).
•The IC substrate should be connected to VDD or float in the PCB layout artwork.
• 80 QFP or bare chip available

CHARACTER PATTERNS

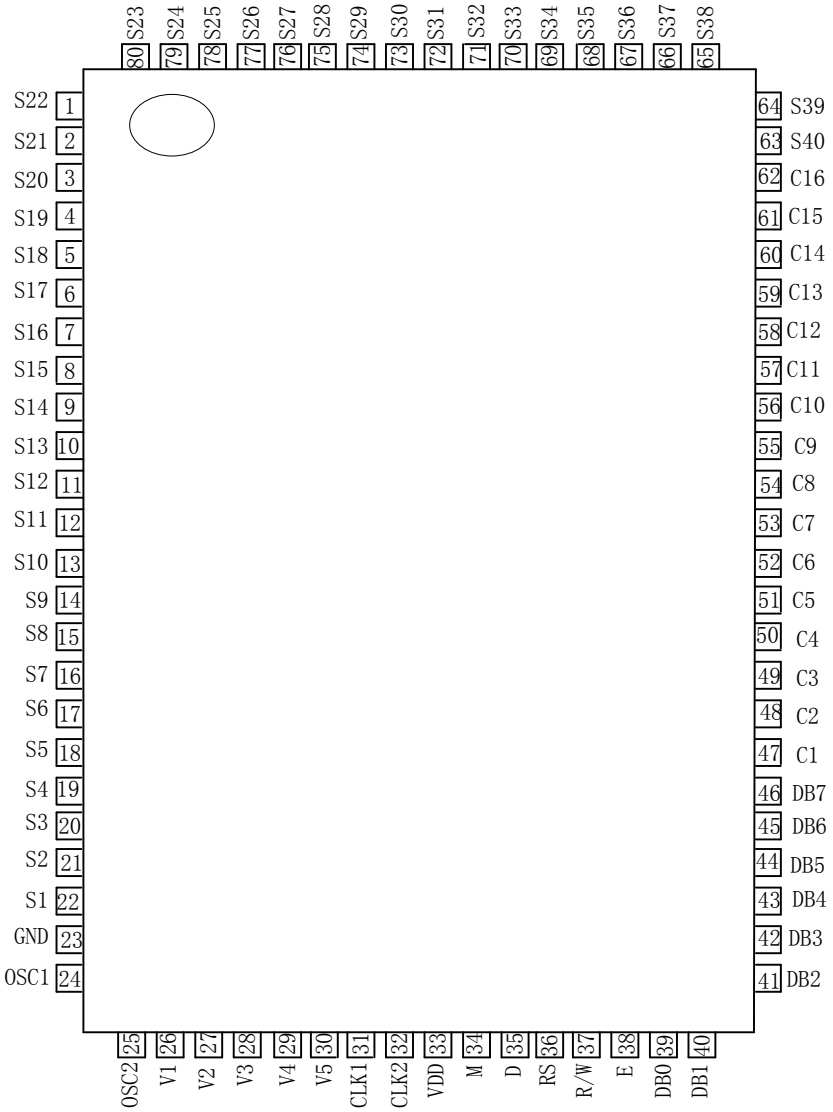
TYPE OF CHARACTER PATTERNS
AIP31066
AIP31066W1
AIP31066W2
AIP31066W3

2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM



2.2、PIN CONFIGURATIONS



2.3、PIN DESCRIPTION

Pin No.	Pin Name		I/O	Description	Interface
33	VDD	Supply Voltage		Supply Voltage for logical circuit (+3V ± 10%,+5V ± 10%)	Power Supply
23	GND			Ground (0V)	
26～30	V1～V5			Bias voltage level for LCD driving	
1～22 63～80	S1～S40	Segment output	O	Segment signal output for LCD drive	LCD
47～62	C1～C16	Common output	O	Common signal output for LCD drive	LCD
24	OSC1	Oscillator	I	Oscillator. When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
25	OSC2		O		
31	CLK1	Extension driver Latch clock	O	Extension driver latch clock	Extension driver
32	CLK2	Extension driver Shift clock		Extension driver shift clock	
34	M	Alternated signal for LCD driver output		Outputs the alternating signal to convert LCD driver waveform to AC.	
35	D	Display data interface		Outputs extension driver data (the 41st dot's data)	
36	RS	Register select	I	Used as register selection input. When RS = “High”, Data register is selected. When RS = “Low”, Instruction register is selected.	MPU
37	R/W	Read/Write	I	Used as read/write selection input. When RW = “High”, read operation. When RW = “Low”, write operation.	
38	E	Read/Write enable	I	Used as read/write enable signal.	
39～42	DB0～DB3	Data bus 0-7	I/O	In 8-bit bus mode, used as low order bidirectional data bus. In 4-bit bus mode, open these pins.	
43～46	DB4～DB7		I/O	In 8-bit bus mode, used as high order bidirectional data bus. In 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output.	

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Power Supply Voltage(1)	VDD	-0.3 ~ +7.0	V
Power Supply Voltage(2)	V_{LCD}	VDD-15.0 ~ VDD+0.3	V
Input Voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	C
Storage Temperature	T_{STG}	-55 ~ +125	C

NOTE: Voltage greater than above may damage the circuit. VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5

3.2、ELECTRICAL CHARACTERISTICS

3.2.1、DC Characteristics (VDD = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	-	4.5	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (VDD=5.0 V, fosc = 270 kHz)	-	0.35	0.6	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	2.2	-	VDD	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	VDD-1.0	-	VDD	V
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH}= -0.205 mA	2.4	-	-	V
	V_{OL1}	I_{OL}= 1.2 mA	-	-	0.4	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O= -40 mA	0.9VDD	-	-	V
	V_{OL2}	I_O= 40 mA	-	-	0.1VDD	
Voltage Drop	Vd_{COM}	I_O=± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN}= 0 V to VDD	-1	-	1	mA
Input Low Current	I_{IL}	V_{IN}= 0 V, VDD= 5 V (PULL UP)	-50	-125	-250	
Internal Clock (external Rf)	f_{OSC1}	Rf = 91 kΩ± 2% (VDD= 5 V)	190	270	350	kHz

External Clock	f_{OSC}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	ms
LCD Driving Voltage	V_{LCD}	VDD-V_5(1/5, 1/4 Bias)	3.0	-	13.0	V

3.2.2、DC Characteristic (VDD =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	-	2.7	-	4.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (VDD=3.0 V, fosc = 270 kHz)	-	0.15	0.3	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	0.7VDD	-	VDD	V
	V_{IL1}	-	-0.3	-	0.55	
Input Voltage (2) (OSC1)	V_{IH2}	-	0.7VDD	-	VDD	V
	V_{IL2}	-	-	-	0.2VDD	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH}= -0.1 mA	0.75VDD	-	-	V
	V_{OL1}	I_{OL}= 0.1 mA	-	-	0.2VDD	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O= -40 mA	0.8VDD	-	-	V
	V_{OL2}	I_O= 40 mA	-	-	0.2VDD	
Voltage Drop	Vd_{COM}	I_O= ±0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN}= 0 V to VDD	-1	-	1	mA
Input Low Current	I_{IL}	V_{IN}= 0 V, VDD= 3 V (PULL UP)	-10	-50	-120	
Internal Clock (external Rf)	f_{OSC1}	Rf = 75 kΩ± 2% (VDD= 3 V)	190	270	350	kHz
External Clock	f_{OSC2}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R ,t_F		-	-	0.2	ms
LCD Driving Voltage	V_{LCD}	VDD-V5 (1/5, 1/4 Bias)	3.0	-	13.0	V

LCD Driving Voltage

Power	Duty	1/8, 1/11 Duty	1/16 Duty
	Bias	1/4 Bias	1/5 Bias
VDD		VDD	VDD
V1		$VDD-V_{LCD}/4$	$VDD-V_{LCD}/5$
V2		$VDD-V_{LCD}/2$	$VDD-2V_{LCD}/5$
V3		$VDD-V_{LCD}/2$	$VDD-3V_{LCD}/5$
V4		$VDD-3V_{LCD}/4$	$VDD-4V_{LCD}/5$
V5		$VDD-V_{LCD}$	$VDD-V_{LCD}$

3.2.3、AC Characteristics (VDD = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-1)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	t_w	230	-	-	
	R/W and RS Setup Time	t_{su1}	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	t_{su2}	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-2)	E Cycle Time	t_c	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	t_w	230	-	-	
	R/W and RS Setup Time	t_{su}	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

3.2.4、AC Characteristics (VDD =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-1)	E Cycle Time	t_c	1000	-	-	ns
	E Rise / Fall Time	t_R ,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	t_{su1}	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	t_{su2}	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-2)	E Cycle Time	t_c	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	t_w	450	-	-	
	R/W and RS Setup Time	t_{su}	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

3.2.5、AC Characteristics (VDD =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Interface Mode with Extension Driver (Refer to Fig-3)	Clock Pulse Width (High, Low)	t_c	800	-	-	ns
	Clock Rise / Fall Time	t_R, t_F	-	-	25	
	Clock Setup Time	t_{su1}	500	-	-	
	Data Setup Time	t_{su2}	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{DM}	-1000	-	1000	

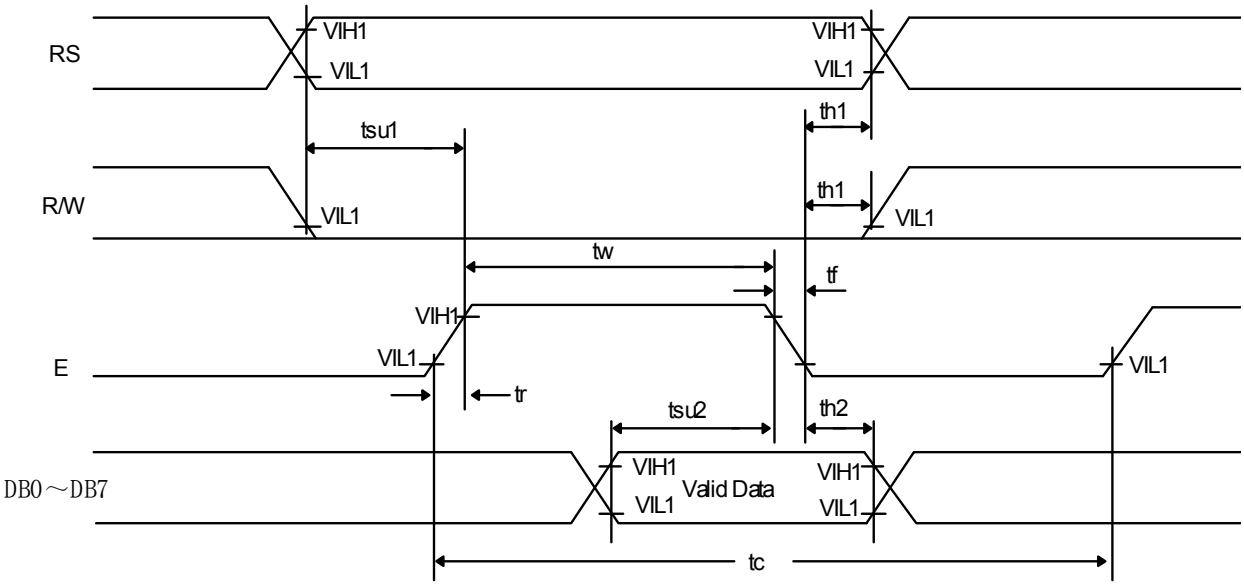


Figure 1 . Write Mode Timing Diagram

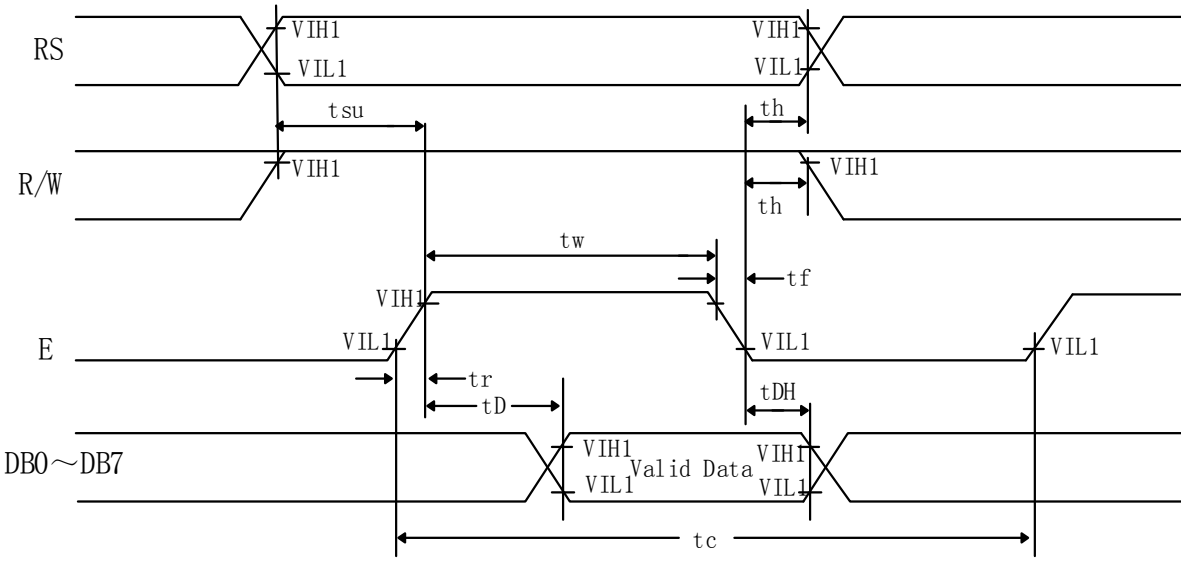


Figure 2 . Read Mode Timing Diagram

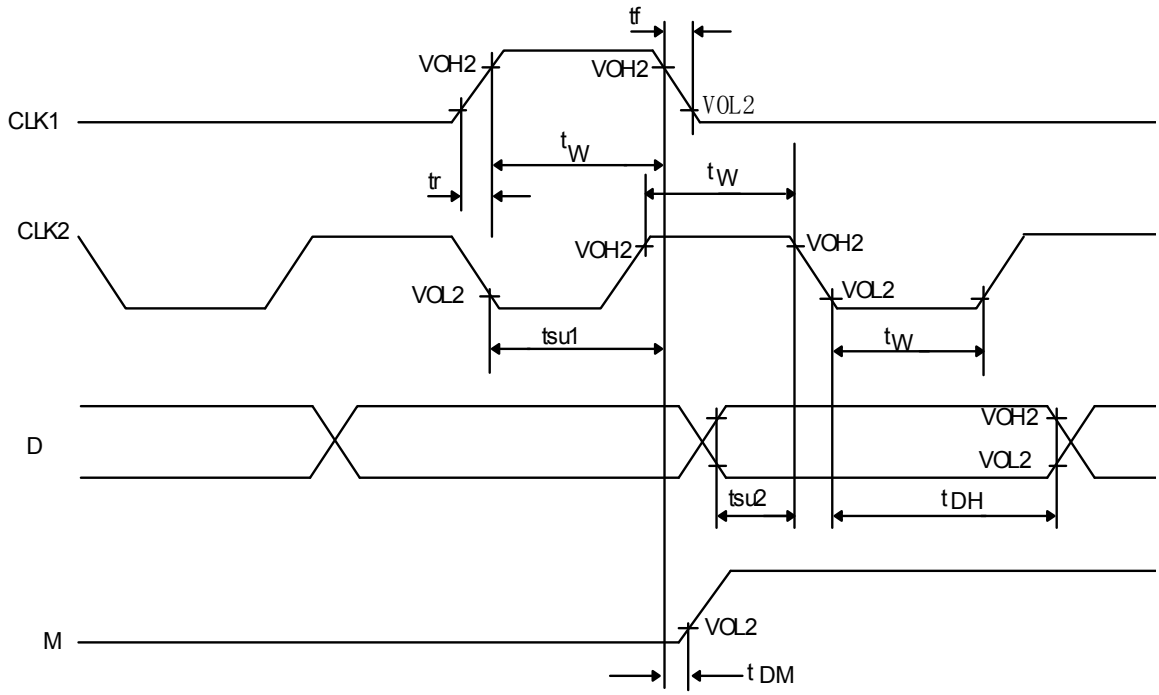
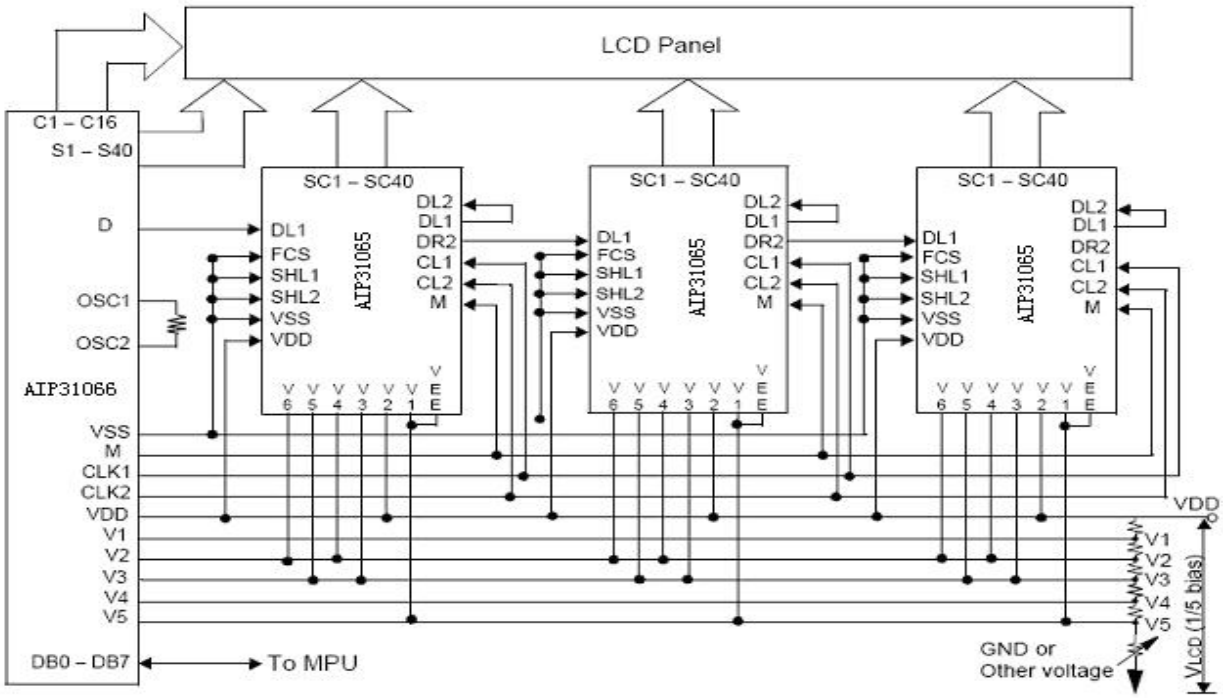


Figure 3 . Interface Mode With Extension Driver Timing Diagram

4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT



4. 2、APPLICATION NOTE

4. 2. 1、FUNCTION DESCRIPTION

- **System Interface**

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.

4-bit bus and 8-bit bus are selected by the DL bit in the instruction register. During read or write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data. To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

Various kinds of Operations according to RS and R/W bits

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy flag(DB7) and address counter (DB0 to DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

- **Busy Flag (BF)**

BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = “Low” and R/W = “High” (Read Instruction Operation). Before executing the next instruction, be sure that BF is not “High”.

- **Address Counter (AC)**

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = “Low” and R/W = “High”, AC can be read through ports DB0 to DB6.

- **Display Data RAM (DDRAM)**

DDRAM stores display data of maximum 80×8 bits (80 characters). DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-4.)

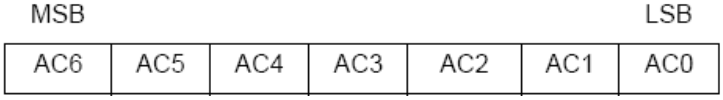


Figure 4 . DDRAM Address

1) 1-line display

In case of 1-line display, the address range of DDRAM is 00H~4FH.

An extension driver will be used. Fig-5 shows the example with 40 segment extension driver added.

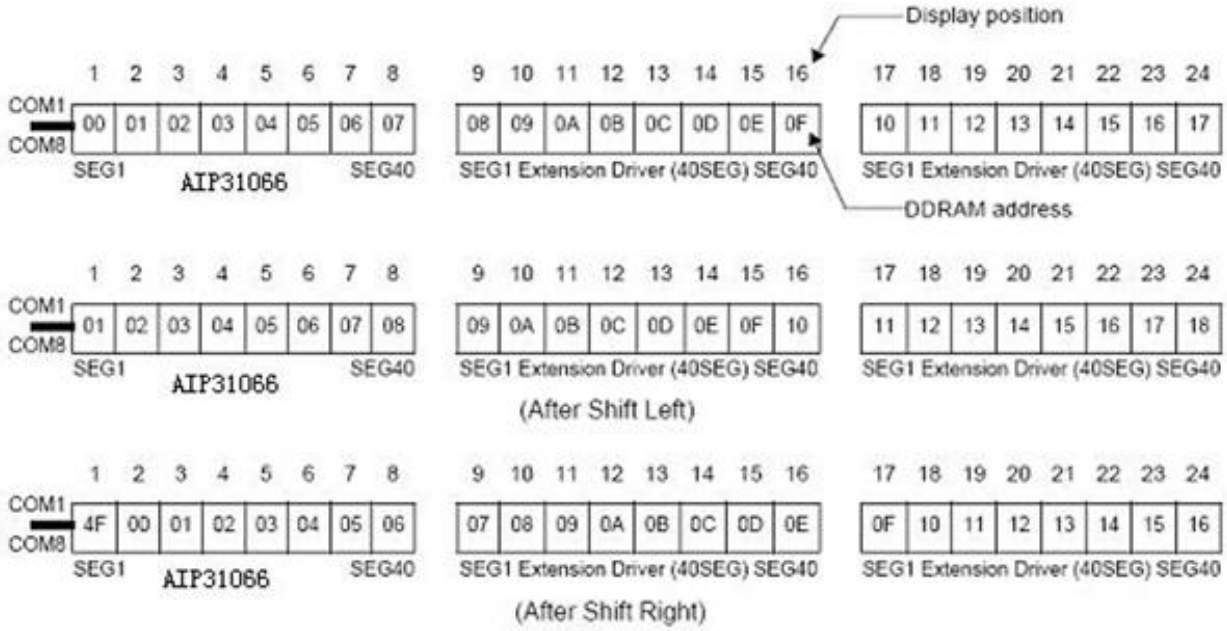


Figure 5 . 1-line × 24 char. display with 40 SEG. extension driver

2) 2-line display

In case of 2-line display, the address range of DDRAM is 00H~27H and 40H~67H.

An extension driver will be used. Fig-6 shows the example with 40 segment extension driver added.

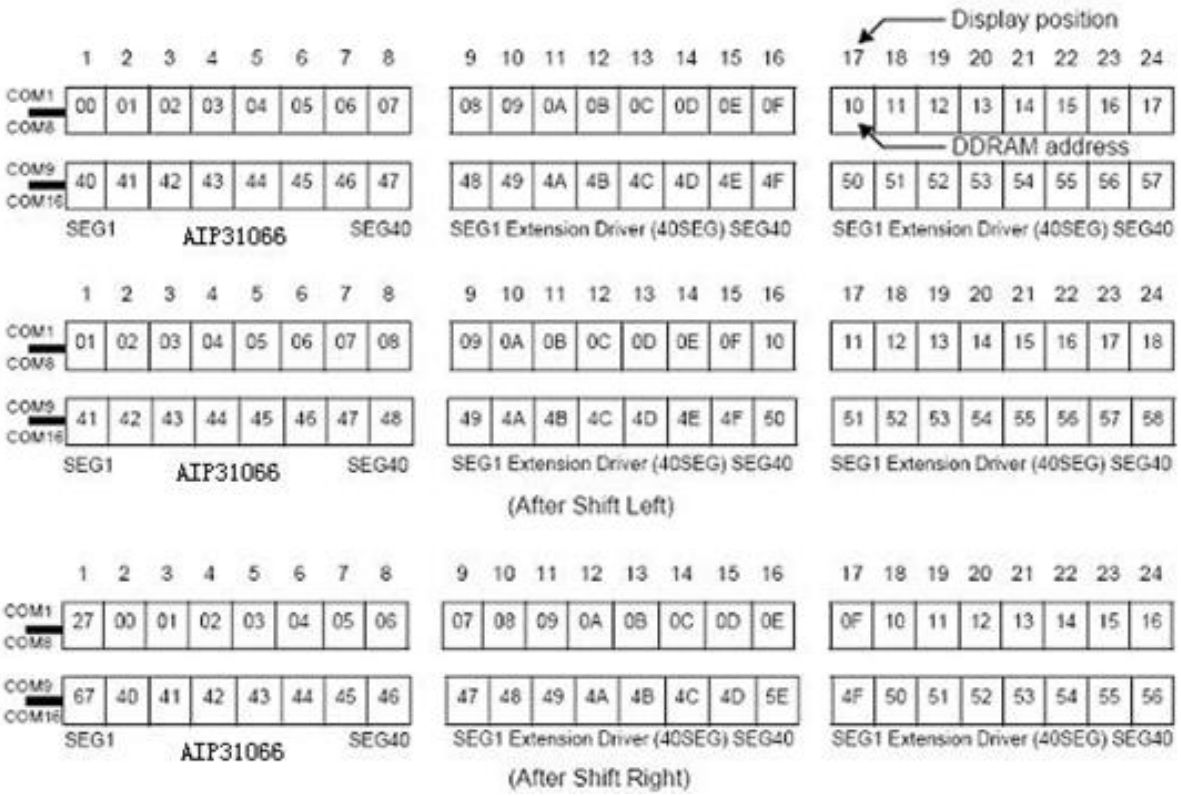


Figure 6 . 2-line × 24 char. display with 40 SEG. extension driver

- **CGROM(Character Generator ROM)**

  CGROM has a 5×8 dots 204 characters pattern and a 5×11 dots 32 characters pattern.

  CGROM has 204 character patterns of 5× 8 dots, and 32 character patterns of 5×11 dots.

- **CGRAM(Character Generator RAM)**

  CGRAM has up to 5×8 dots 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to Table 1)

- **Timing Generation Circuit**

  Timing generation circuit generates clock signals for the internal operations.

- **LCD Driver Circuit**

  LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to a 40-bit segment latch serially, and then is stored to 40-bit shift latch. When each common is selected by 16-bit common register, segment data is also output through segment driver from a 40-bit segment latch. In case of 1-line display mode, COM1 to COM8 have 1/8 duty or COM1 to COM11 have 1/11 duty, and in 2-line mode, COM1 to COM16 have a 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

  It controls the cursor/blink ON/OFF at cursor position.

Table 1. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0	1	1	1	0	pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	×	1	1	1	0	0	0	0	0	0	×	×	×	1	0	0	0	1	pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

4.2.2、INSTRUCTION DESCRIPTION

To overcome the speed difference between the internal clock of AIP31066 and the MPU clock, AIP31066 performs internal operations by storing control informations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 3).

Instructions can be divided largely into four groups:

1) AIP31066 function set instructions (set display methods, set data length, etc.)

2) address set instructions to internal RAM

3) data transfer instructions with internal RAM

4) others

The address of the internal RAM is automatically increased or decreased by 1.

Note: During internal operation, Busy Flag (DB7) is read “High”.

Busy Flag check must be preceded by the next instruction.

When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to “Low”.

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D = “High”).

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

* “-”: dont care

Return Home is cursor return home instruction. Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = “Low”, shifting of entire display is not performed. If SH = “High” and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = “High”: shift left, I/D = “Low”: shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D = “High”, entire display is turned on.

When D = “Low”, display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit

When C = “High”, cursor is turned on.

When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit

When B = “High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B = “Low”, blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data.(Refer to Table 2) During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

Table 2. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N = “Low”, 1-line display mode is set.

When N = “High”, 2-line display mode is set.

F: Display font type control bit

When F = “Low”, 5 ×8 dots format display mode is set.

When F = “High”, 5 ×11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = Low), DDRAM address is from “00H” to “4FH”. In 2-line display mode (N = High), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether AIP31066 is in internal operation or not.

If the resultant BF is “High”, internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not Yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

Table 3. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc= 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5×11dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

* "-": dont care

NOTE: When an MPU program with checking the Busy Flag(DB7) is made, it must be necessary 1/2Fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

4.2.3、INTERFACE WITH MPU

1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

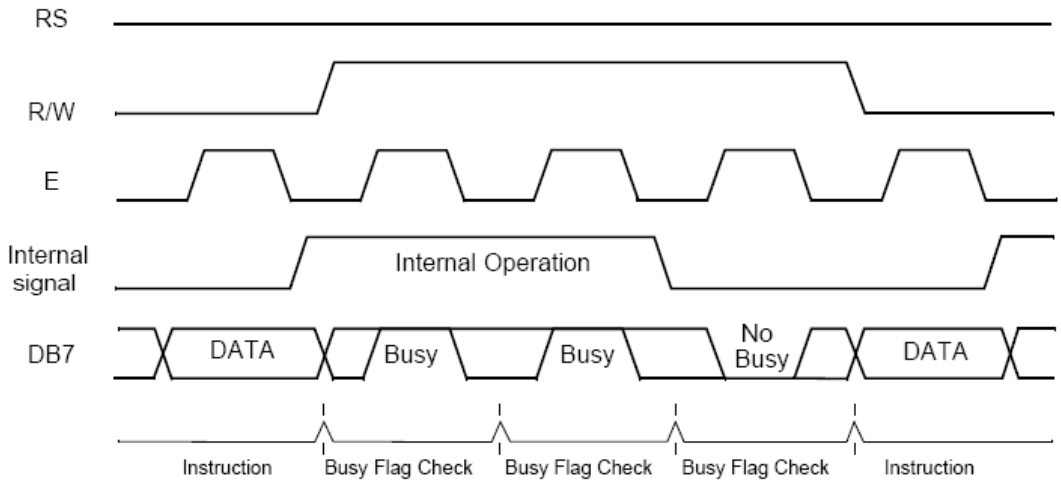


Figure 7 . Example of 8-bit Bus Mode Timing Diagram

2) Interface with 4-bit MPU

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.

At First, the higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7), and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed twice Busy Flag outputs “High” after the second transfer is ended.

Example of timing sequence is shown below.

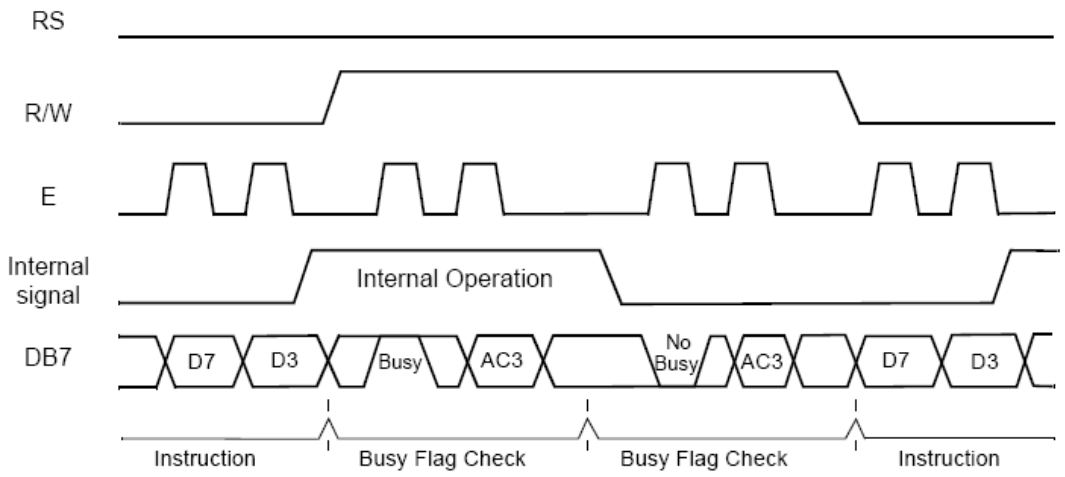
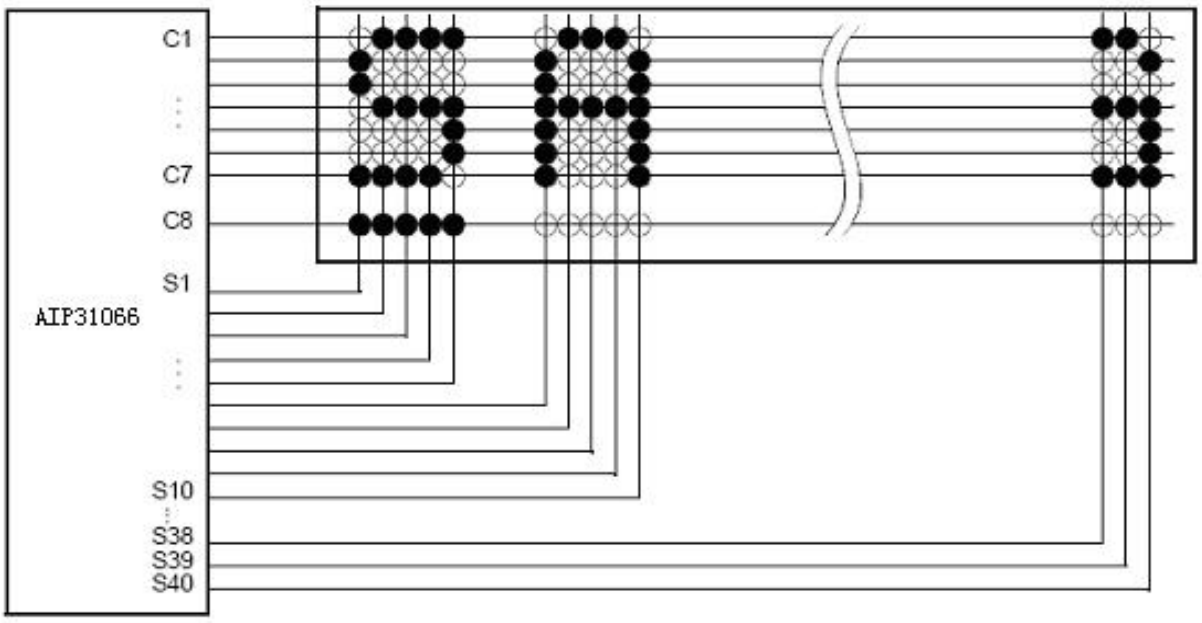


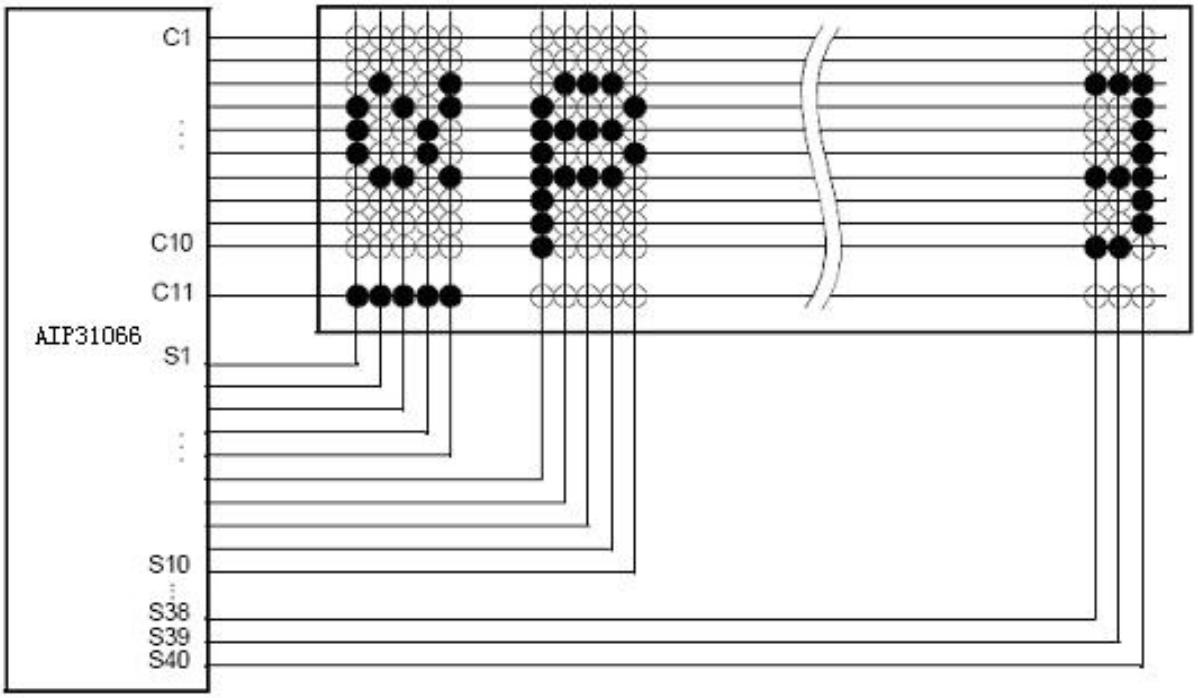
Figure 8 . Example of 4-bit Bus Mode Timing Diagram

4.2.4、TYPACAL APPLICATION

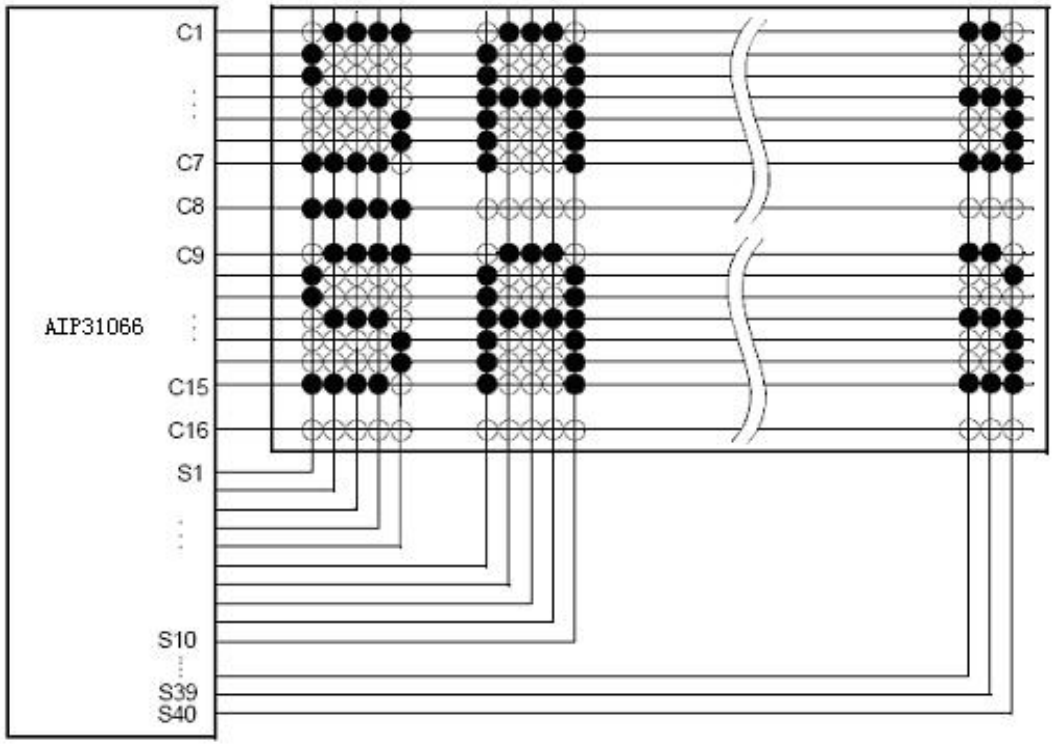
1) LCD Panel: 8 characters ×1-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



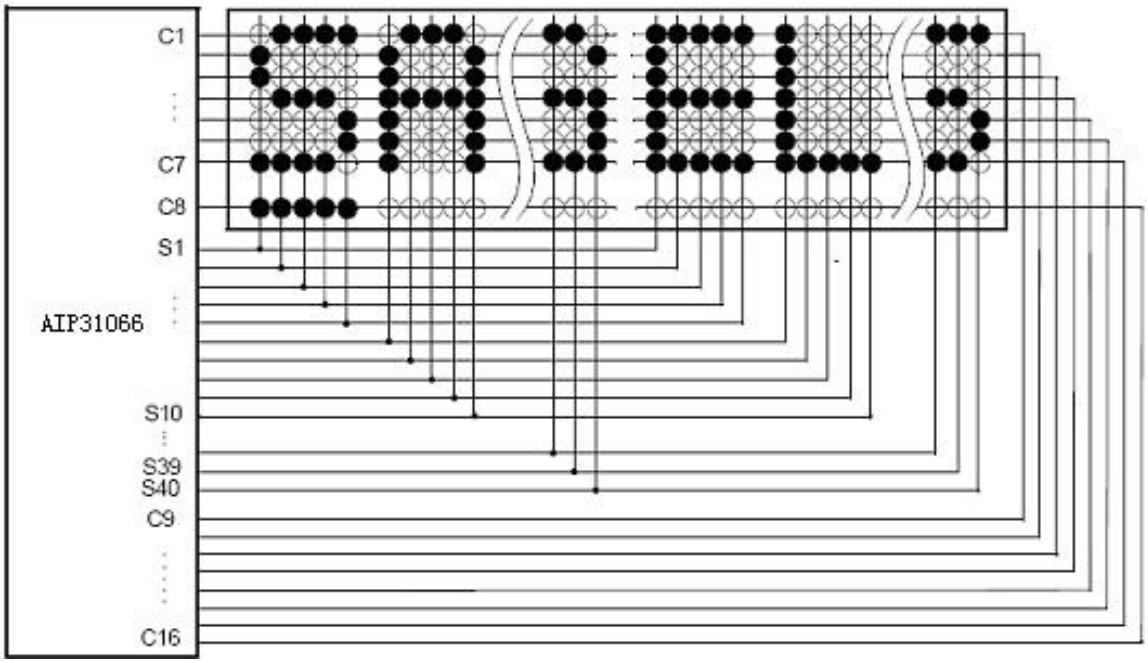
2) LCD Panel: 8 characters ×1-line format (5×10 dots + 1cursor line, 1/4 bias, 1/11 duty)



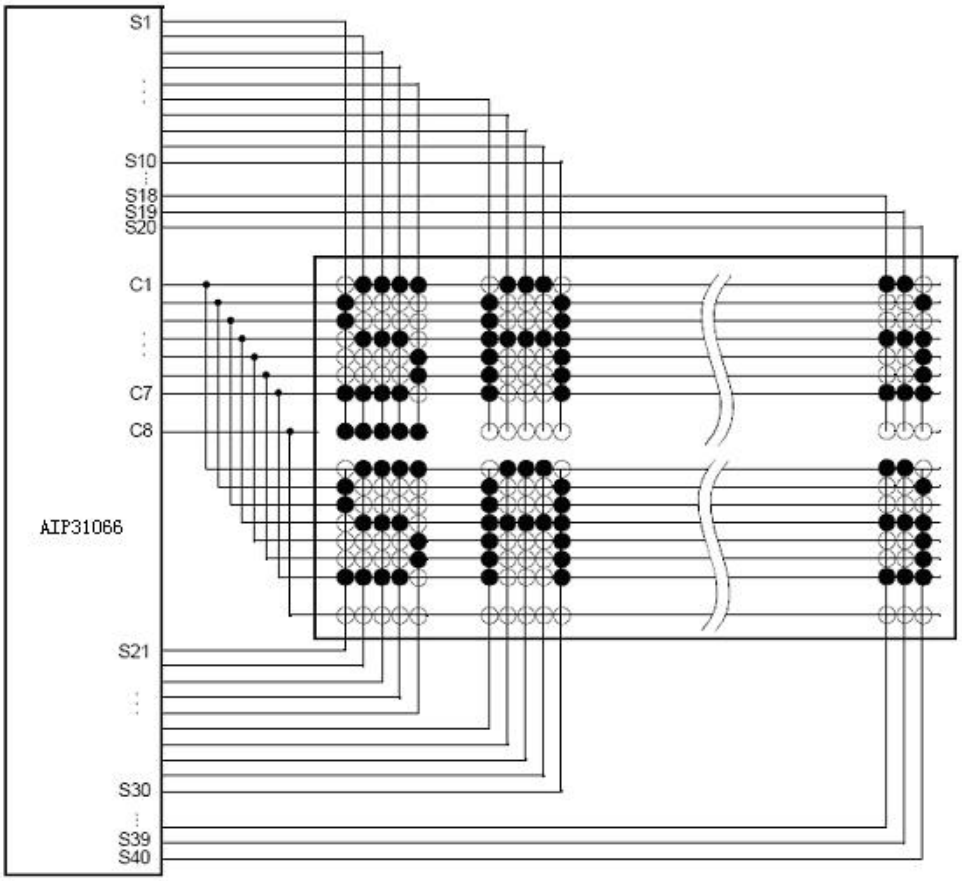
3) LCD Panel: 8 characters ×2 -line format (5×7 dots + line, 1/5 bias, 1/16 duty)



4) LCD Panel: 16 characters ×1-line format (5×7 dots + 1cursor line, 1/5 bias, 1/16 duty)

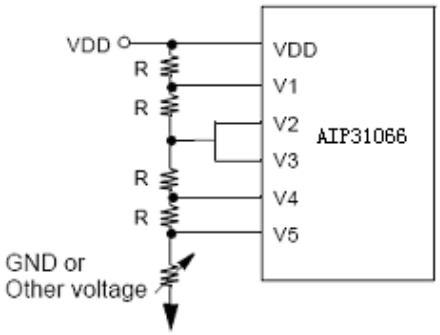


5) LCD Panel: 4 characters ×2-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)

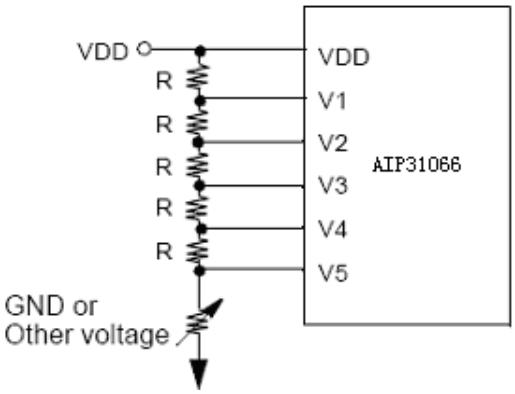


4.2.5、BIAS VOLTAGE DIVIDE CIRCUIT

- 1/4 bias, 1/8 or 1/11 duty



- 1/5 bias, 1/16 duty



4. 2. 6、INITIALIZING

When the power is turned on, AIP31066 is initialized automatically by power on reset circuit.

During the initialization, the following instructions are executed, and BF (Busy Flag) is kept “High” (busy state) to the end of initialization.

(1) Display Clear instruction: Write “20H” to all DDRAM

(2) Set Functions instruction: DL = “High”: 8-bit bus mode

N = “Low”: 1-line display mode

F = “Low”: 5 X 8 font type

(3) Control Display ON/OFF instruction: D = “Low”: Display OFF

C = “Low”: Cursor OFF

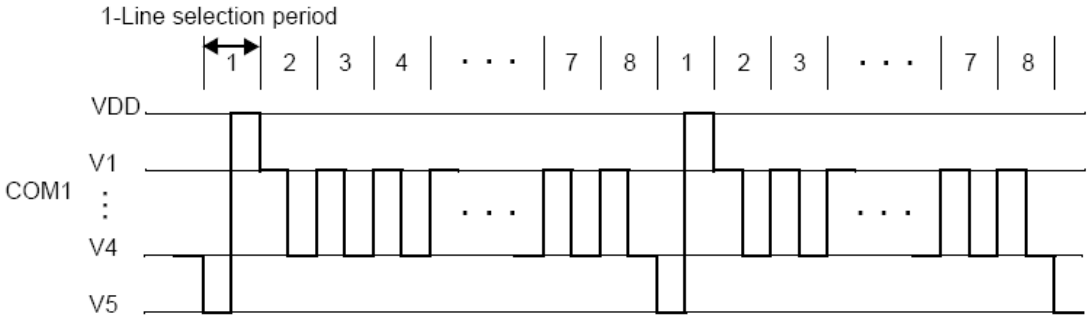
B = “Low”: Blink OFF

(4) Set Entry Mode instruction: I/D = “High”: Increment by 1

SH = “Low”: No entire display shift

4. 2. 7、FRAME FREQUENCY

1) 1/8 duty cycle

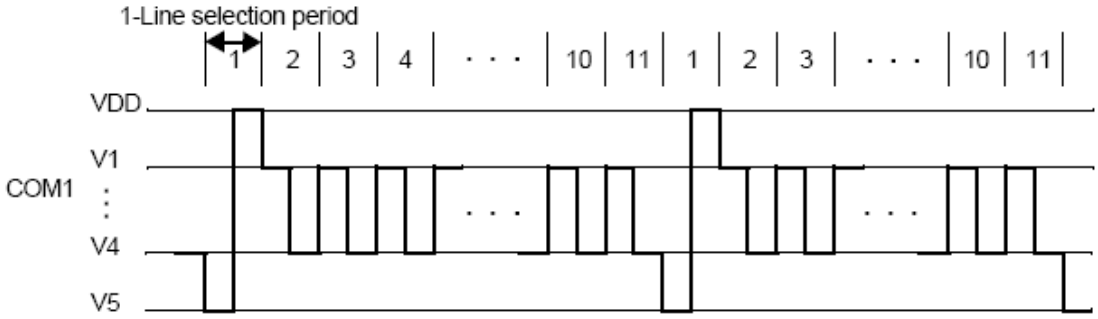


1-Line selection period = 400 clocks

1 Frame = 400×8×3.7 μs = 11850 μs = 11.9 ms (1 clock=3.7 μs, fosc=270 kHz)

Frame frequency = 1 / 11.9 ms = 84.4 Hz

2) 1/11 duty cycle

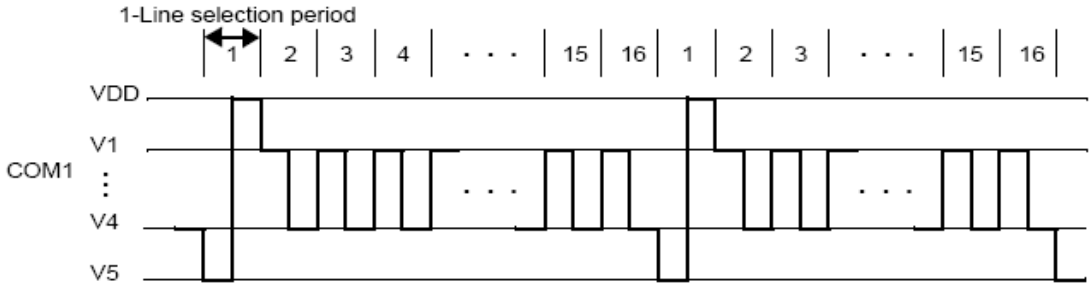


1-Line selection period = 400 clocks

1 Frame = 400×11×3.7 μs = 16300 μs = 16.3 ms (1 clock=3.7 μs, fosc=270 kHz)

Frame frequency = 1 / 16.3 ms = 61.4 Hz

3) 1/16 duty cycle



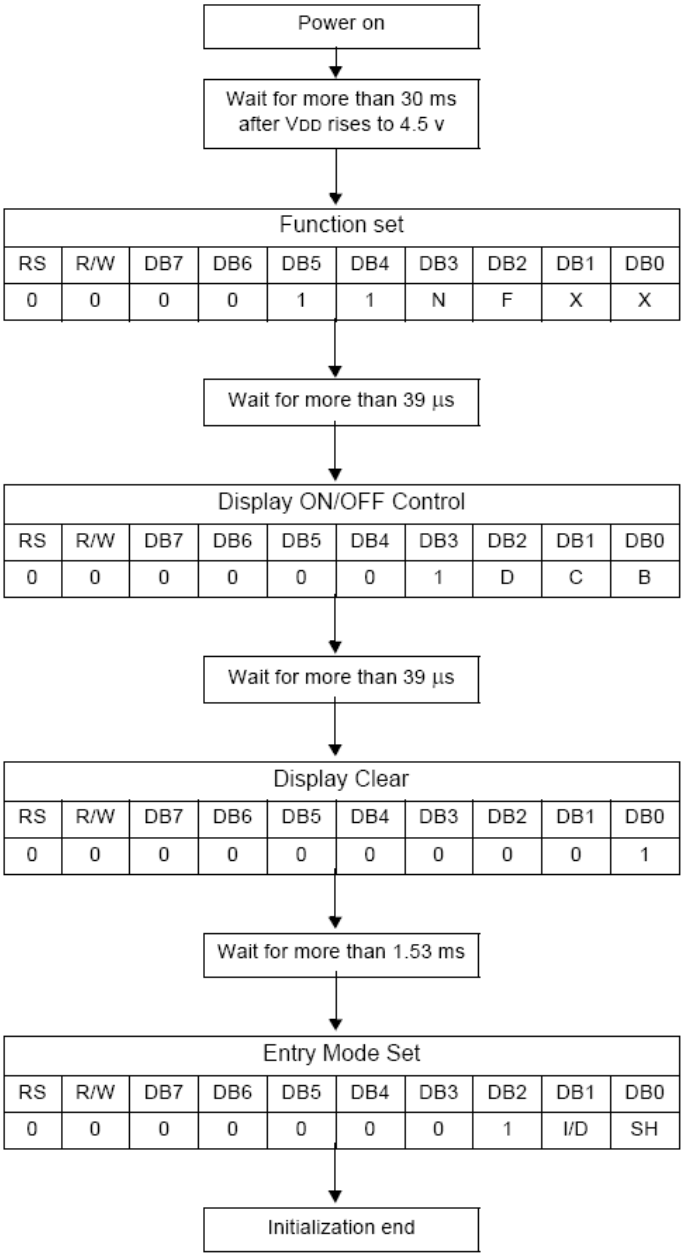
1-Line selection period = 200 clocks

1 Frame = 200×16×3.7 μs = 11850 μs = 11.9 ms (1 clock=3.7 μs, fosc=270 kHz)

Frame frequency = 1 / 11.9 ms = 84.3 Hz

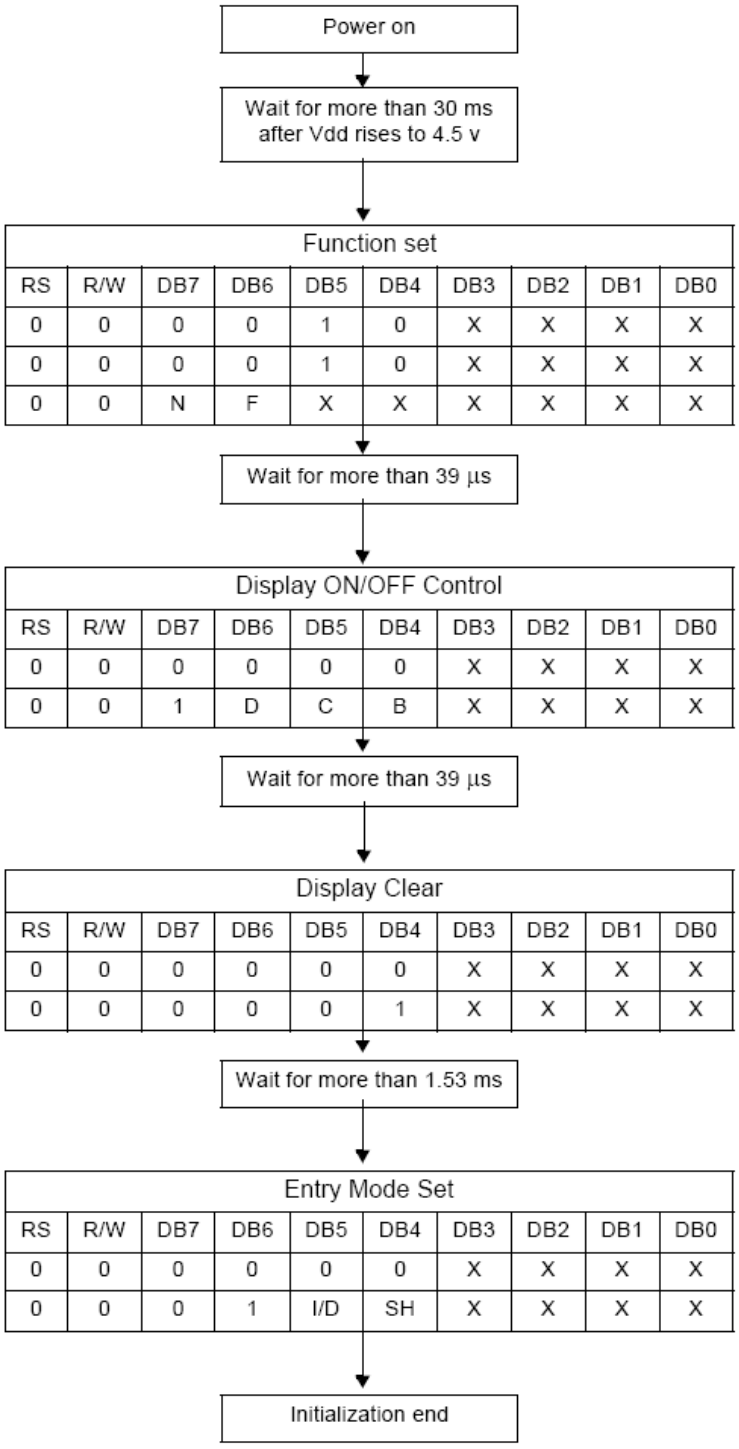
4.2.8、INITIALIZING BY INSTRUCTION

1) 8-bit interface mode (Condition: fosc = 270KHZ)



N	0	1-line mode
	1	2-line mode
F	0	display off
	1	display on
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on
I/D	0	decrement mode
	1	increment mode
SH	0	entire shift off
	1	entire shift on

2) 4-bit interface mode (Condition: fosc = 270KHZ)



N	0	1-line mode
	1	2-line mode

F	0	display off
	1	display on

D	0	display off
	1	display on

C	0	cursor off
	1	cursor on

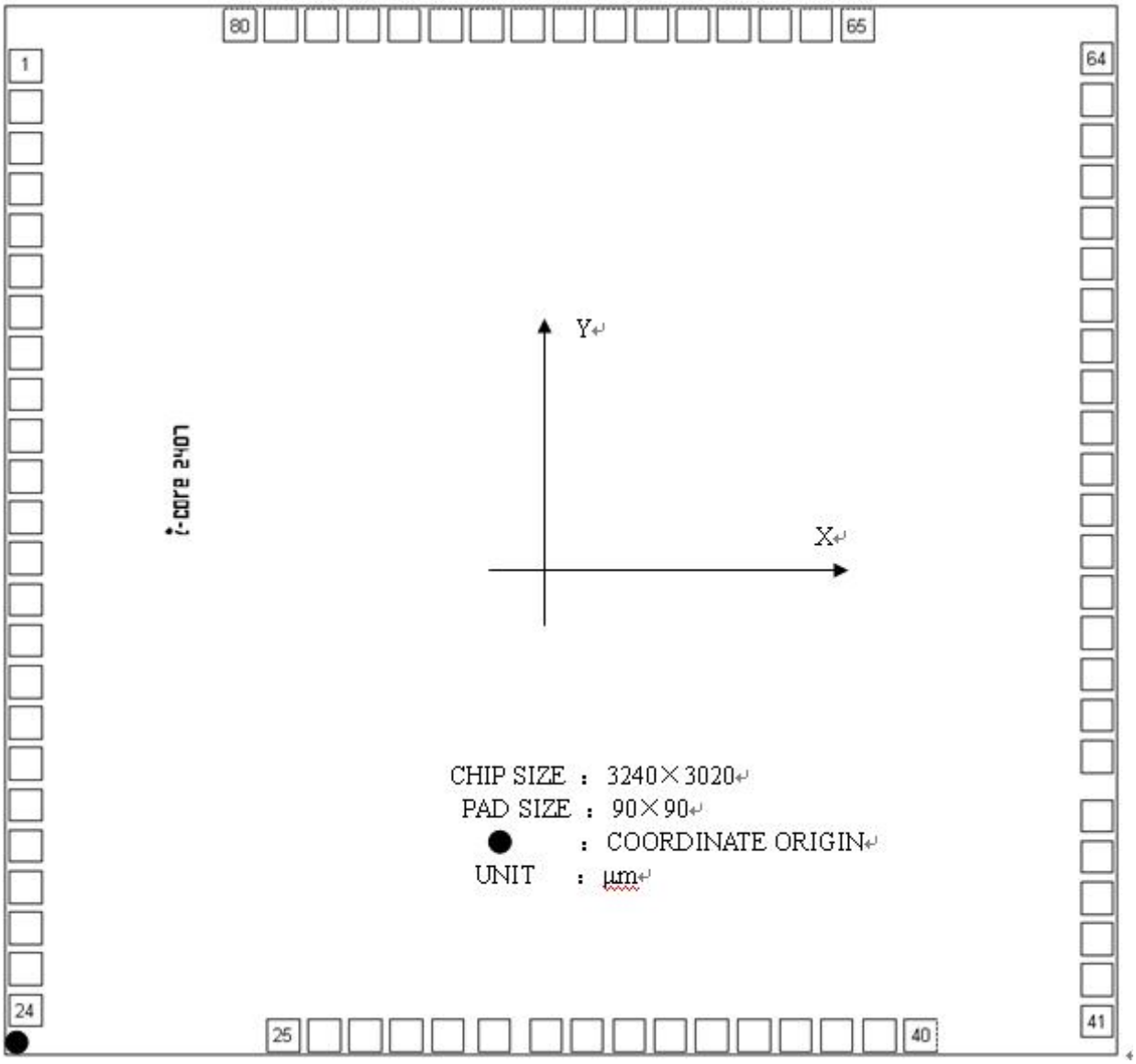
B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM

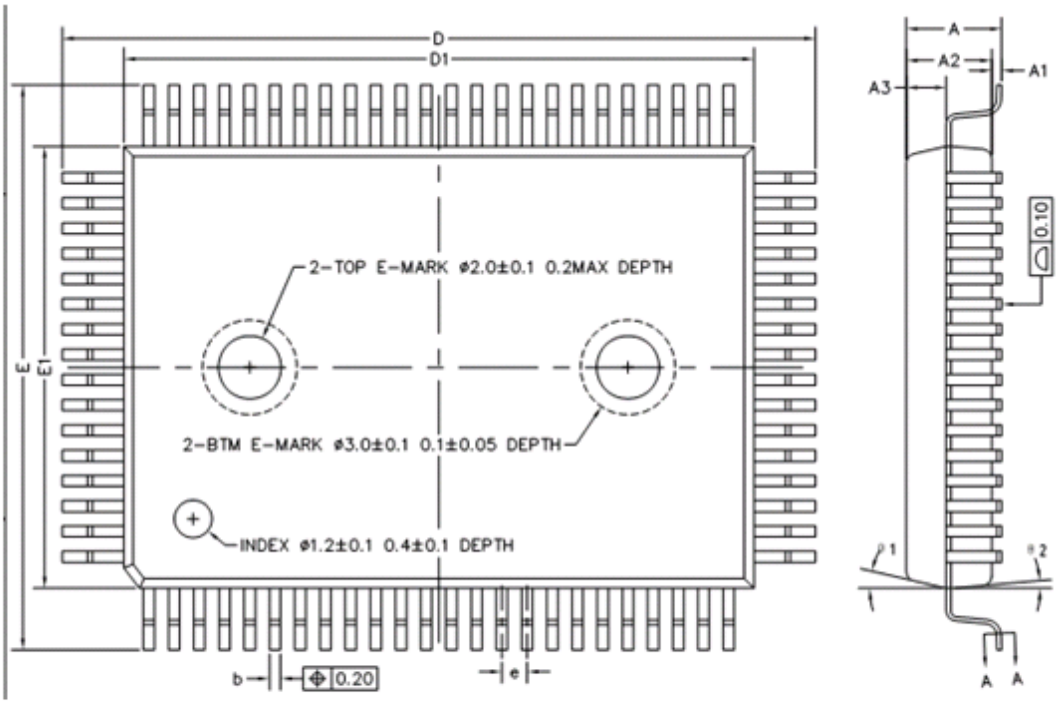


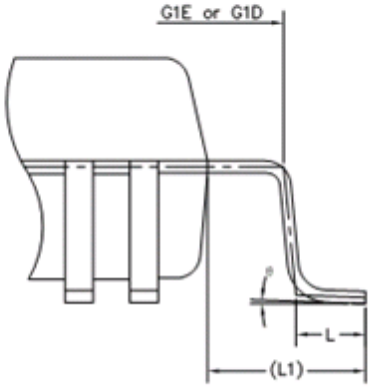
5.2、PAD Location （UNIT:μm）

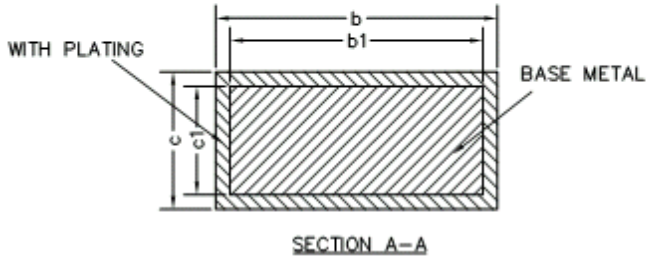
NO.	NAME	X	Y	NO.	NAME	X	Y
1	S22	55.1	2769.8	41	DB2	3046.9	94.6
2	S21	55.1	2654.8	42	DB3	3046.9	209.6
3	S20	55.1	2539.8	43	DB4	3046.9	324.6
4	S19	55.1	2424.8	44	DB5	3046.9	439.6
5	S18	55.1	2309.8	45	DB6	3046.9	554.6
6	S17	55.1	2194.8	46	DB7	3046.9	669.6
7	S16	55.1	2079.8	47	C1	3046.9	835.4
8	S15	55.1	1964.8	48	C2	3046.9	950.4
9	S14	55.1	1849.8	49	C3	3046.9	1065.4
10	S13	55.1	1734.8	50	C4	3046.9	1180.4
11	S12	55.1	1619.8	51	C5	3046.9	1295.4
12	S11	55.1	1504.8	52	C6	3046.9	1410.4
13	S10	55.1	1389.8	53	C7	3046.9	1525.4
14	S9	55.1	1274.8	54	C8	3046.9	1640.4
15	S8	55.1	1159.8	55	C9	3046.9	1755.4
16	S7	55.1	1044.8	56	C10	3046.9	1870.4
17	S6	55.1	929.8	57	C11	3046.9	1985.4
18	S5	55.1	814.8	58	C12	3046.9	2100.4
19	S4	55.1	699.8	59	C13	3046.9	2215.4
20	S3	55.1	584.8	60	C14	3046.9	2330.4
21	S2	55.1	469.8	61	C15	3046.9	2445.4
22	S1	55.1	354.7	62	C16	3046.9	2560.4
23	GND	55.1	239.7	63	S40	3046.9	2675.4
24	OSC1	55.1	124.7	64	S39	3046.9	2790.4
25	OSC2	773.7	55.1	65	S38	2377.6	2882.8
26	V1	888.7	55.1	66	S37	2262.6	2882.8
27	V2	1003.7	55.1	67	S36	2147.6	2882.8
28	V3	1118.7	55.1	68	S35	2032.6	2882.8
29	V4	1233.7	55.1	69	S34	1917.6	2882.8
30	V5	1363.4	55.1	70	S33	1802.6	2882.8
31	CLK1	1507.4	55.1	71	S32	1687.6	2882.8
32	CLK2	1622.4	55.1	72	S31	1572.6	2882.8
33	VDD	1740.3	55.1	73	S30	1457.6	2882.8
34	M	1855.3	55.1	74	S29	1342.6	2882.8
35	D	1970.3	55.1	75	S28	1227.6	2882.8
36	RS	2089.4	55.1	76	S27	1112.6	2882.8
37	R_W	2204.4	55.1	77	S26	997.6	2882.8
38	E	2319.4	55.1	78	S25	882.6	2882.8
39	DB0	2438.8	55.1	79	S24	767.6	2882.8
40	DB1	2553.8	55.1	80	S23	652.6	2882.8

6、PACKAGE INFORMATION

6.1、QFP80



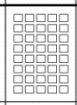
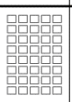
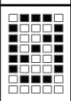
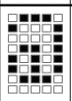
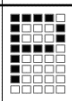
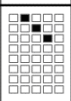
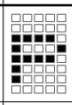
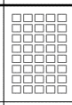
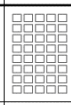
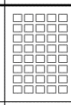
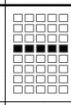
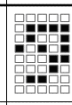
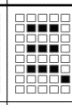
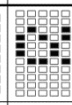
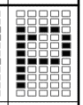
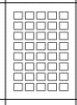
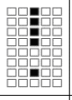
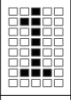
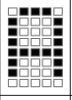
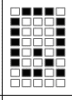
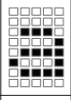
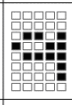
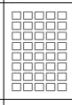
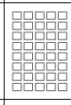
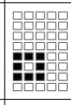
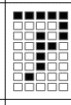
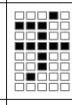
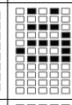
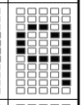
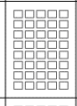
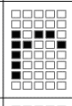
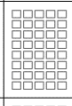
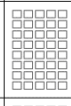
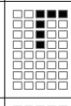




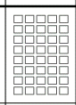
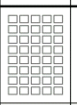
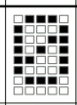
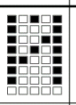
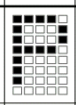
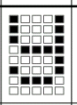
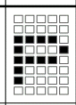
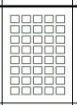
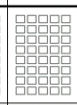
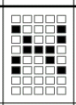
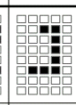
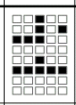
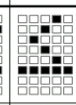
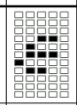
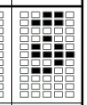
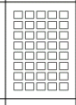
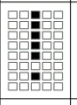
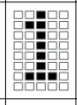
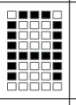
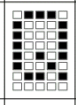
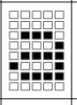
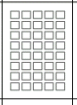
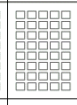
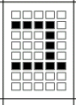
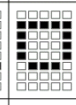
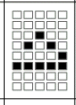
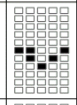
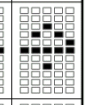
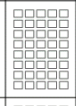
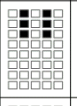
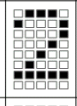
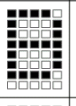
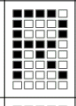
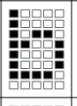
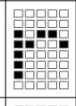
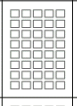
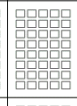
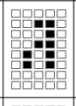
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.32	–	0.42
b1	0.32	0.35	0.38
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.70	0.80	0.90
G1D	22.00REF		
G1E	16.00REF		
L	0.60	0.80	1.00
L1	1.95REF		
θ	0°	2°	8°
θ1	11°	13°	15°
θ2	3°	5°	7°

AIP31066 CHARACTER PATTERNS

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLLL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

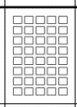
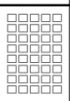
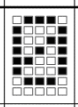
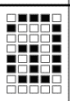
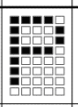
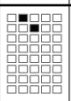
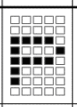
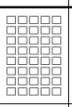
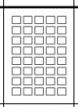
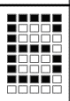
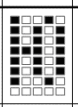
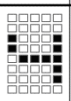
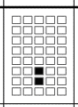
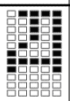
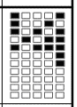
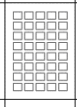
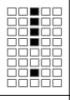
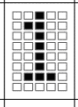
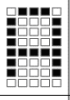
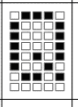
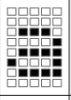
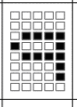
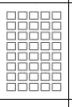
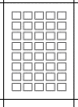
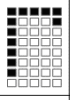
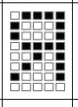
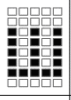
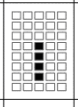
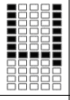
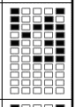
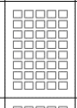
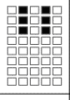
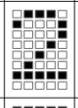
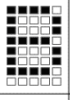
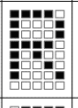
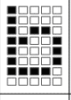
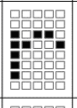
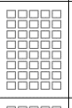
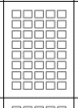
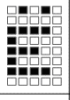
AIP31066W1 CHARACTER PATTERNS

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

AIP31066W2 CHARACTER PATTERNS

Upper 4bit / Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														

AIP31066W3 CHARACTER PATTERNS

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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